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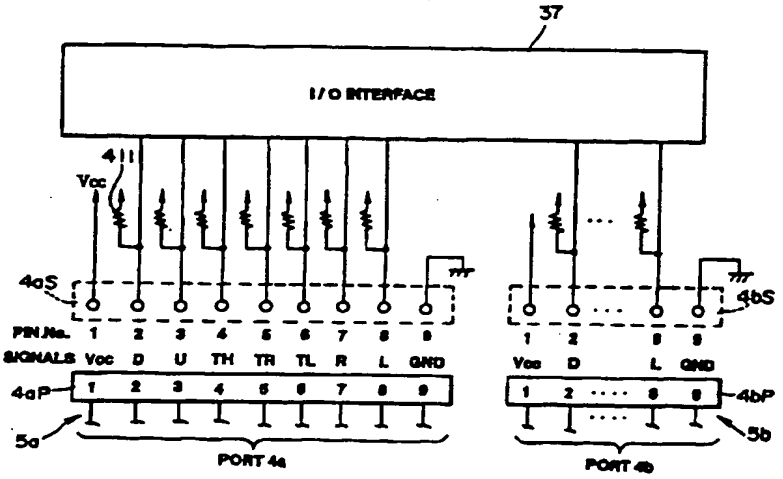
(57) Abstract

A peripheral device for use with a data processing apparatus. The apparatus has a peripheral port with a set of terminal pins consisting of first to ninth pins disposed in a row. The first pin is assigned for one of a power source and the ground potential, the ninth pin for the other of the power source and the ground potential, the second, third, seventh and eighth pins for transmitting data signals, and the fourth to sixth pins for transmitting control signals. The apparatus has an element for selecting the communication mode of the peripheral device connected to the peripheral port, based on the data signals transmitted from the second, third, seventh and eighth pins. The peripheral device comprises a plug connector detachably connected to the peripheral port, the plug connector having a set of terminal pins consisting of first to ninth pins disposed in a row, a cable including a plurality of wires connecting the terminal pins of the plug connector with terminals on an internal printed circuit board, and an element for ransmitting data signals including identification data representing the communication mode via at least one of the second, third, seventh and eighth pins in synchronization with a clock signal supplied from the apparatus.



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SPECIFICATION

IMPROVEMENT IN COMMUNICATION BETWEEN DATA PROCESSING APPARATUS AND PERIPHERAL DEVICE THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an improvement in communication between a data processing apparatus and a peripheral device to be connected to the data processing apparatus, and more specifically, to a system for identifying communication modes of the peripheral devices connected to a game apparatus and connector configurations suitable to the peripheral devices with various types of communication modes.

Description of Related Art

An image processing system is known as a system which has a display such as a television set, (hereinafter, referred to as a "monitor"), on which images are time-dependently displayed. As is widely known for home use, a game apparatus is one representative of such image processing systems.

The game apparatus comprises a processing unit executing game programs and generating video and audio signals. To the apparatus are connected various types of peripheral devices (frequently, referred to as mere "peripherals") such as manipulating switching assemblies called joy pad, controller, or key board. The processing unit mainly performs not only a predetermined image processing

therein but also a variety of processings including control of the peripheral devices. The peripheral devices are used, for example, for inputting necessary information from an operator into the processing unit and for displaying image data such as graphic and character data supplied from the processing unit. The peripheral devices thus typically include an operator controller and a monitor having a screen and speaker.

When the processing unit to which the monitor and operator controller are connected is activated by a player or an operator, the monitor is able to display images on its screen and to produce sound from its speaker, depending on instructions of a given game software sent from the processing unit. The player can enjoy the game with the game apparatus.

The game apparatus is normally required to be able to carry out various games. This means that there is much possibility that various types of peripheral devices are connected to the processing unit.

Various interfaces are arranged between the processing unit and the peripheral devices in aid of communication therebetween. Further, because communication modes are often varied depending on the peripheral device, the processing unit is required to obtain information (peripheral identification data) representing the type of a connected peripheral device. For this requirement, it is proposed that the type of a connected peripheral device can be identified using logical values acquired through data lines of the peripheral device when the processing unit sends twice the

peripheral device a peripheral selection signal of logical values of "1" firstly, and then of "0". Such prior art is disclosed in Japanese patent Laid-open No.2-62618, for example.

However, the above identification method identifies in fact only the type of a connected peripheral device on the basis of logical values acquired though data lines of the device. In other words, this identification method does not give attention to the communication mode of a connected peripheral device. This results in a drawback that, frequently, connected peripheral devices cannot send data to the processing unit and also the processing unit cannot control the peripheral devices with preferable communication modes to those peripheral devices.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to make it possible for a data processing apparatus to communicate for data transmission employing various types of communication modes with various peripheral devices.

Another object of the present invention is to provide a data processing apparatus adaptable to various types of communication modes.

Still another object of the present invention is to provide a connector plug configuration, which connects a peripheral device to a data processing apparatus adaptable to various types of peripheral devices.

Still another object of the present invention is to provide a

peripheral device having a connector assembly suitable for transmission of control signals and data with a data processing apparatus.

Still another object of the present invention is to provide a data processing apparatus with a system for identifying various types of communication modes of peripheral devices connected to the apparatus.

Still another object of the present invention is to provide a data processing apparatus with a system for controlling various types of peripheral devices connected to the apparatus through a connector with an improved pin configuration.

Still another object of the present invention is to provide a connector used in a peripheral device, the connector incorporating a plug having a terminal pin configuration which efficiently and rapidly transmits to a processing apparatus necessary information in order that the processing apparatus identifies a communication mode inherently given to the peripheral device, thereby a smooth communication being permitted between the processing apparatus and peripheral device on the communication mode.

In order to achieve the objects, according to one aspect of the present invention, there is provided a peripheral device for use with a data processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins and being disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said ninth pin being

assigned for connecting to the other of the power source and the ground potential, said second, third, seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins being assigned for transmitting control signals, said apparatus having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said second, third, seventh and eighth pins, said peripheral device comprising: a plug connector which is to be detachably connected to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins and being disposed in row in the order of the first to the ninth pins correspondingly to said first to ninth pins of the peripheral port; a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device; and means for transmitting data signals including identification data representing the communication mode of said peripheral device via at least one of said second, third, seventh and eighth pins in synchronization with a clock signal supplied from said apparatus when said plug connector is connected to said peripheral port.

According to another aspect of the invention, there is still provided a combination of a data processing apparatus and a peripheral device, comprising: said apparatus having a peripheral port with a plurality of terminal pins disposed in a row, said terminal pins including a pair of first pins, one assigned for connecting to one of a power source and the ground potential and

the other assigned for connecting to the other of the power source and the ground potential, at least one of second pins assigned for transmitting data signals, a plurality of third pins assigned for transmitting control signals, said apparatus further having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said at least one second pin, means for transmitting a clock signal via one of said third pins to said peripheral device and means for performing a communication with the connected peripheral device with the selected communication mode; said peripheral device having a plug connector which is to be detachably connected to said peripheral port, said plug connector having a plurality of terminal pins configured as the same in number as and disposed in a row correspondingly to the terminal pins of said peripheral port, said peripheral device further having a cable including a plurality of wires connecting the terminal pins of said plug connector with terminal on a printed circuit board of said peripheral device and means for transmitting data signals including identification data representing the communication mode of said peripheral device via said at least one of second pin to said apparatus in synchronization with said clock signal when said plug connector is connected to said peripheral port.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

Fig. 1 is a perspective illustration of a game system embodying

the present invention;

Fig. 2 is a basic block diagram showing the game system;

Fig. 3 is a block diagram showing the connection between a main CPU and a sub CPU functioning as a system for managing and controlling peripheral devices and showing the block diagram of the sub CPU;

Fig. 4 shows a connector configuration of peripheral ports;

Figs. 5A to 5C are pin configurations of plug connectors employed in compliance with typical communication modes;

Figs. 6A to 6D are functional block diagrams of typical controllers as peripheral devices;

Figs. 7A to 7D are detailed circuit diagrams of typical controllers as peripheral devices;

Fig. 8 is a flowchart exemplifying a processing carried out by the sub CPU;

Fig. 9 is a flowchart of an access subroutine to peripheral devices;

Fig. 10 shows a flowchart of an access subroutine for a three-wire handshake type of communication mode;

Fig. 11 shows a flowchart of an access subroutine for a clocked parallel type of communication mode;

Fig. 12 is a flowchart of an access subroutine for a clocked serial type of communication mode;

Fig. 13 represents a timing chart of control signals and data for the three-wire handshake type of communication mode;

Fig. 14 represent a timing chart of control signals and data for

the clocked parallel type of communication mode; and

Fig. 15 is a timing chart of control signals and data for the clocked serial type of communication mode.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of the present invention will now be explained with reference to Figs. 1 to 15.

Fig. 1 shows a perspective view of a game system 1 to which the present invention is applied. The game system 1 comprises a game apparatus 2 functioning as the data processing apparatus for processing game programs and controlling various operations and control switch assemblies or controllers 3a and 3b as an example of peripheral devices to the game apparatus. As for the controllers, such control keys disclosed in U. S. patent application S. N. 08/245,446 may be used. The apparatus 2 is provided with connector ports 4a and 4b for connecting peripheral devices. Each of the connector ports 4a and 4b has a socket or a socket connector 4as(4bs) to which a plug or a plug connector 4ap(4bp) can be connected and disconnected.

The plugs 4ap and 4bp are connected to the controllers 3a and 3b through cables 5a and 5b, respectively. The controllers 3a and 3b are electrically and functionally connected to internal circuits of the game apparatus 2 via the cables 5a and 5b when the plugs 4ap and 4bp are inserted into the sockets 4as and 4bs.

Each of the plugs 4ap and 4bp has a configuration of plug pins which ensures transmission of a communication mode employed for

the controllers 3a and 3b to the game apparatus 2. Further, the apparatus 2 comprises a video output terminal and an audio output terminal not shown.

The video output terminal is connected to a video input terminal 7a of a monitor 6, such a television set, through a cable 8a. Also the audio output terminal is connected to an audio input terminal 7b of the monitor 6 through a cable 8b.

The game apparatus 2 has a CD-ROM drive block 14 positioned at the central portion thereof. The CD-ROM drive block 14 is installed with a CD-ROM drive 9 and an optical pickup to read game program data or audio/video software from CD-ROM discs mounted thereto. The apparatus is further provided with a cartridge port 10 positioned at the rear side of the CD-ROM drive block 9. The cartridge port portion 10 is installed therein with a socket connector to which are connected devices such as a ROM/RAM cassette or an optional adapter for providing additional functions (not shown).

The apparatus 2 carries out a wide variety of information processings and controls such as image processings, audio processings and control of peripheral devices as well as processing of game programs. The controllers 3a and 3b provide the apparatus 2 operating signals. A video and audio signals generated by the apparatus 2 are given to the monitor 6 through the cables 8a and 8b.

Fig. 2 exemplifies a block diagram of the game apparatus 2. The apparatus 2 shown therein comprises a processing block 11, video block 12, audio block 13, and auxiliary block or CD-ROM drive

block 14. The cartridge port 10 includes a cartridge interface (I/F) 15 and the auxiliary block 14 includes a compact disk interface (I/F) 16.

The processing block 11 comprises a main processing unit (CPU) 21, RAM 22, ROM 23, system control unit 24, and sub CPU 25. The main CPU 21 is functionally connected, via a bus line 26, to the RAM 22, ROM 23, system control unit 24, and sub CPU 25.

Through the bus line 26, system control unit 24 and a bus line 17, the main CPU 21 is functionally connected with the video block 12, audio block 13, cartridge I/F 15, and CD I/F 16. The CD I/F 16 of the auxiliary block 14 is connected with the CD-ROM drive 9.

The main CPU 21 controls the entire processings of the system. In order to enhance control capability, the main CPU 21 consists of 32-bit RISC types high speed CPUs (two CPU chips called SH-2) and provides an improved, high speed calculating operation which may function similarly as a digital signal processor (DSP).

RAM 22 has, for example, a memory capacity of 32 megabits in all, a memory area of 16 megabits of which is assigned to the main CPU 21, for example. The remaining memory area of the RAM 22 is assigned to the video block 12 and audio block 13. ROM 23 stores initial programs or bootstrap programs for the hardware and for the cassette ROM and the CD-ROM.

The system control unit 24 functions as a co-processor to the main CPU 21 so that the unit 24 interfaces 16-bit bus 17 to which the video block 12, audio block 13 and auxiliary block 14 are connected with 32 bit bus 26 to which the main CPU 21 is

connected.

When the electric power is on and/or a reset button is pushed down, the sub CPU 25 not only resets the entire system but also carries out data collection from the peripheral devices such as the controllers 3a and 3b to control the peripheral devices. Also the sub CPU 25 can change the clock frequency of the entire system.

The sub CPU 25 further includes a connection-exchanging means described below. The connection-exchanging means selectively connects the peripheral devices such as the controllers 3a and 3b connected to the connector ports 4a and 4b with either a CPU core 31 (refer to Fig. 3) in the sub CPU 25 or the main CPU 21.

The video block 12 forms video signals on the basis of video control signals given from the main CPU 21 through the system control unit 24 and provides the monitor 6 the video signals through the cable 8a. This permits the monitor 6 to display images on its screen. The details of the video block 12 may be referred to PCT/JP94/01068 (filed Feb. 24, 1995 in U. S.), PCT/JP94/01067 (filed Feb. 27, 1995 in U. S.), PCT/JP94/01066 (filed Feb. 27, 1995 in U. S.).

The audio block 13 generates digital audio signals on the basis of audio control signals given from the main CPU 21 through the system control unit 24, converts those digital audio signals into corresponding analog audio signals by a digital/analog (DA) converter incorporated therein, and provides the monitor 6 the converted analog audio signals through the cable 8b. Such processing permits an audio speaker of the monitor 6 to produce

sound.

The sub CPU 25 will be explained with reference to Fig. 3. Fig. 3 represents in block diagram the configuration of the sub CPU 25 which acts as a unit for controlling and managing peripheral devices. As shown in the figure, the sub CPU 25 is coupled with the main CPU 21 by way of the bus line 26. The sub CPU 25 comprises a CPU core 31, ROM 32, RAM 33, register table 34, register group 35, multiplexer 36, and I/O interface 37.

The CPU core 31, for example, may be a 4-bit CPU. The CPU core 31 is coupled with the ROM 32 to receive required programs from the ROM 32. Coupled with the CPU core 31 through a bus line 38 are the RAM 33, register table 34, and the register group 35. Further, the register group 35 is coupled with the I/O interface 37 via the multiplexer 36. The register group 35 and multiplexer 36 compose the connection-exchanging means 40.

The register group 35 may be sub-grouped into a main-CPU register group 351, a sub-CPU register group 352, and an I/O section register 353. The main-CPU register group 351 has two terminals; one is connected with the main CPU 21 through a bus line 39 and the bus line 26, while the other is connected with one of the two exchanging terminals of the multiplexer 36. The sub-CPU register group 352 has also two terminals; one is connected with the CPU core 31 through a bus line 38, while the other is connected with the other of the exchanging terminals of the multiplexer 36.

The multiplexer 36 has a common terminal connected with the

I/O interface 37. The interface I/O 37 is connected with the connector ports 4a and 4b. The connector ports 4a and 4b are connected, through cables 5a and 5b, with the controllers 3a and 3b, respectively.

In response to data specified in the I/O section register 353, the multiplexer 36 functionally connects the peripheral devices such as the controllers 3a and 3b selectively to either the CPU core 31 through the register group 352 and bus line 38 or the main CPU 21 through the register group 351 and bus lines 39 and 26.

The CPU core 31 is designed such that, when the CPU core 31 is electrically connected with the peripheral devices via the multiplexer 36, the CPU core 31 communicates with the peripheral devices in the order of "peripheral ID-1" , "peripheral ID-2", "data size" and "data", decides a communication mode from those IDs(identification data), and then performs collection, transmission and exchanges etc. of the data.

In this embodiment, the data "peripheral ID-1", which consists of 4-bit data, represents a communication mode in accordance with the type of a peripheral device. The data "peripheral ID-2", which also consists of 4-bit data, is a type of data representing the device model of a peripheral device and consists of a set of data showing a device model focusing on signal types showing whether the signal is, for example, analog or digital. The "data size" represents the total bite number of data from a peripheral device and will be shown by references "DSIZE0 to DSIZE3" in figures described below. The "data" represents data, which are supplied

from a peripheral device, of the total bite number specified by the "data size". The CPU core 31 reads the data having the above total number at every 4-bit, because the CPU core 31 is a 4-bit processor in this embodiment.

Although the register group 35, multiplexer 36 and I/O interface 37 have two-channel circuits, respectively, this embodiment shows only one-channel circuit for simplified explanation.

Details of sub CPU 25 may be referred to co-pending Japanese patent applications Nos.6-246579 and 6-246580.

As shown in Fig. 4 the I/O interface has two channels connected to peripheral ports 4a and 4b. Each of the peripheral ports 4a and 4b has a set of socket pins 1 through 9. Pins 2 through 8 are connected to I/O interface and assigned to send and receive a set of specific signals. Names and functions of the signals are shown in Table 1.

As shown in Fig. 4, each of plugs 4ap and 4bp which are to be connected to the sockets 4as and 4bs respectively has a set of plug pins 1 through 9 corresponding to the socket pins 1 through 9. The plug 4ap and 4bp are connected to main circuits of peripheral devices via cables 5a and 5b.

Table 1

Signal Name	Pin No.	Remarks
TH	4	Control signal from game apparatus
TR	5	Control signal from game apparatus
TL	6	Control signal to game apparatus(ack)
R	7	Data signal (third bit)
L	8	Data signal (second bit)
D	2	Data signal (first bit)
U	3	Data signal (0-th bit)
Vcc	1	Power Source(+5V)
GND	9	GND

Pins nos. 4 to 6 are assigned for control signals. Pin no. 4 is the first control pin and assigned for transmitting a peripheral selection signal TH from the game apparatus 2 to the peripheral device (for example, controllers 3a, 3b). Pin no. 5 is the second control pin and assigned for transmitting a data request signal TR from the game apparatus to the peripheral device. Pin no. 6 is the third control pin and assigned for transmitting a peripheral acknowledgement signal TL from the peripheral device to the game apparatus.

Pins nos. 2, 3, 7 and 8 are assigned for data signals. Pin no. 2 (the first data pin) is assigned for transmitting a bit data D, pin no.

3 (the second data pin) for a bit data U, pin no. 7 (the third data pin) for a bit data R, and pin no. 8 (the fourth data pin) for a bit data L, respectively. The data R is mainly used for data transmission to the game apparatus 2. The input/output directions of data for these signals D, U, R and L can optionally be specified in accordance with the kind of the peripheral device connected to the apparatus 2. The signal R represents the third bit of the data, L the second bit, D the first bit and U the 0-th bit, respectively.

Pins 2 through 8 are connected to an electric power source Vcc by way of resisters 411, respectively, thereby to pull up the voltage levels of the signal lines (pins nos. 2 to 8) to the level of the power source Vcc.

When a peripheral device is not connected to the port 4a (4b) the voltage level on each of pins nos. 2 to 8 is equal to the voltage value of the power source Vcc (i.e. logical value = binary value "1"). Thus, the sub CPU 25 identifies that a peripheral device is not connected to the socket 4as (4bs) when it receives these data of the voltage state "1", for example, for D, U, R and L.

Pins nos. 5 and 6 are mainly assigned for transmitting control signals between the game apparatus and the peripheral devices in the above description. However, pins 5 and 6 may be used for data signal transmission where a peripheral device employs either the clocked parallel communication mode or clocked serial communication mode which will be described below.

Pin no. 1 is assigned to the signal Vcc which represents the power source (voltage: +5V). The pin no. 9 is assigned to the signal

GND which represent the ground potential (voltage: zero).

Figs. 5A to 5C explain a variety of pin configurations for plugs 4ap and 4bp which vary depending on communication modes employed by peripheral devices. Fig. 5A shows a pin configuration for standard communication modes including a TH/TR-selection communication mode and a three-wire handshake communication mode, Fig. 5B shows a pin configuration for a clocked parallel communication mode (clock-synchronized-type parallel communication mode), and Fig. 5C shows a pin configuration for a clocked serial communication mode (clock-synchronized-type serial communication mode), respectively. The clocked parallel and serial communication modes correspond to the non-standard type of modes.

These pin configurations are prepared to easily comply with a large number of types of peripheral devices, such as a control PAD, mouse, key board, modem and memory unit, and with different communication modes which may change according to peripheral devices.

Typical communication modes employed by a variety of peripheral devices are, for example, a TH/TR-selection communication mode, a three-wire handshake mode, a clocked parallel mode, and a clocked serial mode. A peripheral device employing the TH/TR-selection and three-wire handshake communication modes requires all of the socket/plug pins 1 through 9 of the connector port 4a (4b) to be used electrically independently. Accordingly, as shown in Fig. 5A, all the pins 1

through 9 of the plug 4ap (4bp) are not short-circuited to each other.

On the other hand, where a peripheral device employs the clocked parallel communication mode, pin no. 5 assigned for the data request signal TR and pin no. 6 assigned for peripheral acknowledgment signal TL can electrically be short-circuited as shown in Fig. 5B. Further, in case of a peripheral device employing the clocked serial communication mode, the data transmission lines in the connector port 4a (4b) can be reduced to one line in principle, and it is possible to transmit data through the one data line in cooperation with the two peripheral selection line (TH) and data request line (TR). Accordingly, as shown in Fig. 5C, pin no. 2 may be connected to Vcc and pins 6 to 8 may be connected to GND.

As is exemplified above, it is understood that each of the connector ports 4a and 4b have a certain requirement in the number of needed signal lines (i.e., pins), which is determined in accordance with the employed communication mode. The processing apparatus 2 can use logical values on specified signal lines (in other words, specified pins) at the connector ports 4a and 4b to decide communication modes. Namely the apparatus 2 can determine the communication modes according to the logical values on the signal lines (pins).

Thus, in order to identify the employed communication mode, it should be essential to know the numbers of pins required to transmit data and the logical values on each signal line (i.e., each specified pin). In the present embodiment, the pin configurations

of the plugs are designed to be able to transmit effectively to the apparatus 2 the logical values required to decide the communication mode employed by a peripheral device. In consequence, the apparatus 2 can quickly decide the employed communication mode.

Where the communication mode of a peripheral device is clocked parallel mode, the pin configuration of each plug 4ap (4bp) of the connectors are shown in Fig. 5B. In this mode, the apparatus 2 transmits to the controllers 3a and 3b a specified logical value ("1" or "0") as the peripheral selection signal TH and given clock signals as the data request signal TR. In response to this, signals of required logical values are then quickly provided through the data lines from the controllers 3a and 3b in synchronization with the clock signals. As shown in Fig. 5B, the pin 5 for the data request signal TR is short-circuited with the pin 6 for the peripheral acknowledgment signal TL in this clocked parallel communication mode, thereby the signals (voltages) on both the plug pins no. 5 and 6 being the same. Accordingly the signal TR transmitted from the apparatus 2 to pin no. 5 is sent back almost simultaneously from pin no. 6 to the apparatus 2 as the signal TL. Thus, the apparatus 2 identifies the clocked parallel mode by sensing signal TL equal to signal TR.

Further, in case of a peripheral device of the clocked serial communication mode, only one signal line (U) is required to transmit data. In addition, only the peripheral selection signal line (TH) and data request signal line (TR) transmitting clock signals

are required as control lines. And logical values needed to identify this communication mode may be set as R=L="0", D="1", and U="1". These requirements may be realized by such pin configurations of the plugs 4ap and 4bp as shown in Fig. 5C in which plug-pins which are not used for transmitting data and control signals are connected to fixed potentials (Vcc and GND). For example, pin no. 2 is connected to the power source Vcc and pins nos. 6 to 8 are connected to the ground GND. This plug-pin configuration will make it possible to produce required logical values representing the clocked serial communication mode at the pins of the plugs 4ap and 4bp, thus such logical values being supplied to the apparatus 2.

The short-circuit between the pins in Figs. 5B and 5C may be achieved either by putting a short-circuit wire bridging connecting portions at which the plug pins are connected to the corresponding wires contained in the cable 5a (or 5b) in the plug or by providing a short-circuit pattern on a printed circuit board arranged in the plug 4ap (4bp). This reduces in number wires in the cable 5a (or 5b) connecting the plug 4ap (4bp) to the main circuit of a peripheral device.

The foregoing short-circuit can be achieved within the main circuit of a peripheral device either by putting a short-circuit wire bridging wires of the cable 5a (or 5b) or by forming a specified short-circuit printing pattern on a printed circuit board. Though this short-circuit design cannot reduce the cable 5a (or 5b) in number, the plug can be reduced in size.

Particularly in the case of pin configuration of the plug 4ap

(4bp) shown in Fig. 5C assigned to the clocked serial communication mode, the no. 2 pin is short-circuited and electrically connected to the no. 1 pin (signal Vcc; power source pin) and the pins nos. 6 to 8 are all short-circuited and electrically connected to the no. 9 pin (signal GND; ground pin). And accordingly wires in the cable connecting the plug 4ap (or 4bp) with the main circuit of a peripheral device can largely be decreased in number, because only the lines of the data signal U and the control signals TH and TL are required.

On one hand, when the pin configuration of Fig. 5C is effectively realized within a peripheral device, the lines of the cable, independent of signal transmission, are electrically connected to the power source and the ground potential, which leads to reduced noises which may fall onto the lines.

The functional and hardware schematic diagrams of controllers as representatives of peripheral devices employing the foregoing various communication modes will now be explained, respectively, with reference to Figs. 6A to 6D and 7A to 7D which use part of the same reference numerals as ones described above.

Fig. 6A shows a controller 3a employing the TH/TR-selection communication mode. The controller 3a comprises the plug connector 4ap, the cable 5a having nine wires connected to the nine plug pin nos. 1 to 9 of the plug connector 4ap, and a main circuit 3M to which the wires of the cable 5a are connected. The nine plug pin nos. 1 to 9 are electrically independent from each other and individually connected to the nine wires of the cable 5a. The main

circuit 3M has an operating portion 3Ma and a data generator 3Mb. The operating portion 3Ma, which is operated by a player, includes keys and/or switches. The data generator 3Mb is formed by circuits such as hardware logic circuits or a CPU system such that a specific group of 4-bit data R, L, D, U including data generated at the operating portion 3Ma are selected from other data groups and supplied through the plug pin nos. 2, 3, 7, 8 in response to bit patterns of both the peripheral selection signal TH and data request signal TR.

One detailed hardware schematic diagram of a controller 3a employing the TH/TR-selection communication mode is exemplified in Fig. 7A. As shown therein, the data generator 3Mb consists of a one chip type logic IC containing buffers and other logic gates such as AND and NAND gates for carrying out the foregoing operation. Various key switches arranged on the top cover of the controller 3a and pushed by a player are connected to the logic IC 3Mb. Among them are a start key "START", 4-way directional keys "UP(I)", "DOWN(I)", "LEFT(I)" and "RIGHT(I)", specialized right- and left-steering keys "T R" and "T L", and other keys "T A" to "T C" and "T X" to "T Z" assigned for special functions such as jumping and rotation in a monitor screen. The logic IC 3Mb selects key data of the above key switches every one group (three keys or four keys are combined as one group) in response to bit patterns of the 2-bit data selecting signals TH and TR (i.e., peripheral selection signal TH and data request signal TR).

Fig. 6B shows a controller 3a employing the three-wire

handshake communication mode. The controller 3a comprises the plug connector 4ap, the cable 5a having nine wires connected to the nine plug pin nos. 1 to 9 of the plug connector 4ap, and a main circuit 3M to which the wires of the cable 5a are connected. The nine plug pins 1 to 9 are electrically independent from each other and individually connected to the nine wires of the cable 5a. The main circuit 3M has an operating portion 3Ma and a CPU system 3Mb. The CPU system 3Mb has a CPU and functions as a data generator which is responsive to the operating portion 3Ma. A data generator formed by hardware logic circuits can be adopted as a substitute for the CPU system. The CPU system 3Mb communicates with the game apparatus 2 using the three signals TH, TR, and TL sequentially inputted or outputted through the plug connector 4ap and then supplies 4-bit parallel data R, L, D, U including data generated at the operating portion 3Ma to the game apparatus 2 through the plug connector 4ap. When output signals from an operating portion 3Ma are analog quantities, the operating portion 3Ma includes signal processing circuits such as an A/D convertor.

For example, one controller 3a employing the three-wire handshake communication mode is shown in detail in Fig. 7B, which has a CPU system 3Mb and executing the foregoing signal processing. The CPU system 3Mb includes IC J1 (part No. 74HC157) which functions as a selector for selecting ID data. The selector includes four of 2-inputs/1-output type selecting circuit connecting to another IC J2 which is a 4-bit microcomputer (CPU). Various key switches operated in a video game, for instance, which

composes the operating portion 3Ma, are connected to IC J2. Thus in response to the peripheral selection signal TH and data request signal TR, the microcomputer not only reply by sending out the peripheral acknowledgement signal TL but also reads the states of the key switches, and outputs them as 4-bit data R, L, D, U by way of IC J1.

Fig. 6C shows a controller 3a employing the clocked parallel communication mode. The controller 3a also comprises the plug connector 4ap of nine pin nos. 1 to 9, the cable 5a, and a main circuit 3M. Among the nine plug pin nos. 1 to 9, the pins of nos. 5 and 6 are short-circuited at their pin portions to each other and the remaining pins are still electrically independent. The plug pins of Nos. 1 to 5 and 7 to 9 are coupled with the respective wires of the cable 5a. The main circuit 3M has an operating portion 3Ma and a data generator 3Mb which can be constructed using gate array circuits, for example. The data generator 3Mb, through the plug connector 4ap, sequentially receives the peripheral selection signal TH and data request signal TR (potentially equal to the peripheral acknowledgement signal TL due to the short circuit) and, almost simultaneously with the reception of the signal TR, supplies to the game apparatus 2 4-bit parallel data including data generated at the operating portion 3Ma. The plug pin configuration of this mode reduces the number of wires of the cable 5a by one, as shown in Fig. 6C. The clocked parallel communication mode permits the game apparatus 2 to communicate with the controller 3a in the same manner as the three-wire handshake mode.

Fig. 7C exemplifies the detailed internal block diagram of a controller 3a employing the clocked parallel communication mode. A data generator 3Mb, which consists of gate arrays, plays a key role for the foregoing operation in the controller 3a. The data generator 3Mb includes ICs J3, J4 (part No. 74HC74) and IC J5 (74HC14) which play together a key role for generating a 3-bit data selecting signal supplied to each of four parallel-arranged ICs J6 to J9. ICs J6 to J9 (part No. 74HC151) are selectors of 8-inputs/1-output type and each arranged to receive key data from each of four-divided key groups in the key switches of the operating portion 3Ma. Each of ICs J6 to J9 selects one data (including ID data or key data) responsibility to bit patterns of the supplied 3-bit data selecting signal (i.e., address signal). Thus, 4-bit parallel data R, L, D, U are outputted from ICs J6 to J9.

Fig. 6D shows a controller 3a employing the clocked serial communication mode. The controller 3a also comprises the plug connector 4ap of nine pins of nos. 1 to 9, the cable 5a, and a main circuit 3M. Among the nine plug pins of nos. 1 to 9, the pins of nos. 1 and 2 are short-circuited and the pins of nos. 6 to 9 are short-circuited, respectively, at their pin portions to each other and the remaining pins are still electrically independent. The plug pins of nos. 1, 3 to 5, and 9 are coupled with the respective wires of the cable 5a. The main circuit 3M has an operating portion 3Ma and a data generator 3Mb which can be constructed using gate array circuits, for example. The data generator 3Mb, through the plug connector 4ap, sequentially receives the peripheral selection signal

TH and data request signal TR, and in response to clock pulse inversion, supplies to the game apparatus 2 serial data including data generated at the operating portion 3Ma. The plug pin configuration of this mode remarkably reduces the number of wires of the cable 5a by four, as shown in Fig. 6D.

Fig. 7D shows one detailed example of a controller 3a employing the clocked serial communication mode. The controller 3a has a data generator 3Mb consisting of gate arrays, where included are ICs J10 to J12 (part No. 74LS166), which are cascade-connected, are shift registers. IC J10 placed at the first stage are used for sending ID data in sequence. ICs J11 and J12 placed at the second and third stages are connected to the key switches of the operating portion 3Ma and used for sending serial key data U. Thus in response to the peripheral selection signal TH and data request signal TR, ICs J11 to J12 sends out ID data and key data in sequence. This controller 3a has facilities for a cascade connection of controllers. In other words, there is provided a circuit J13 for recognizing whether serial data from another cascade-connected controller are inputted through a socket connector 4as'.

In Figs. 6C and 6D, and 7C and 7D, such short-circuit configuration can be achieved in the side of the main circuit 3M.

In the present embodiment, when the plug 4ap (or 4bp) connected to the controller 3a (or 3b) is inserted into the socket 4as (or 4bs) arranged in the apparatus 2, the foregoing plug pin configurations permit the sub CPU 25 to communicate to process in

the order of "peripheral ID-1", "peripheral ID-2", "data size", and "data", even though the controller 3a (or 3b) as the peripheral device adopts different communication modes or different device types. Also the foregoing plug pin configuration provides the communication of "peripheral IDs" and "data" in a proper state, although types and/or communication modes of peripheral devices are different.

The operation of the apparatus 2 functionally including the system for identifying communication modes of peripheral devices will now be explained with reference to Figs. 3 to 15 and Table 2 to 6.

As shown in Fig. 8, after being activated, the sub CPU 25 first outputs the control signals TH="1" and TR="1" (refer to Step S101 in Fig. 7). The CPU core 31 of the sub CPU 25 reads logical values of the data signals R, L, D and U produced on pins 7, 8, 2 and 3 by each of the peripheral devices and stores the read logical values into a predetermined memory area of the RAM 33 (Step S102). The CPU core 31 again outputs the control signals TH="0" and TR="1" (Step S103). In response to this, the CPU core 31 again reads logical values of the data signal R, L, D and U produced by the peripheral devices and stores them into a predetermined memory area of the RAM 33 (Step S104: see the intervals T_{10} in Fig. 12 and T_{20} in Fig. 13).

The CPU core 31 then calculates the "peripheral ID-1" (Step S105). The "peripheral ID-1" can be calculated using the following formula.

[ID-1] = {(data R in TH="1") or (data L in TH="1")} x 8h
+ {(data D in TH="1") or (data U in TH="1")} x 4h
+ {(data R in TH="0") or (data L in TH="0")} x 2h
+ {(data D in TH="0") or (data U in TH="0")} x 1h

, where h represents suffix for hexadecimal number. Using the calculated results of [ID-1], the CPU core 31 identifies the types of peripheral devices (Steps S106 to S110). The following table 2 shows a relation between the types of peripheral devices and the calculated results of [ID-1].

Table 2

Peripheral Device	ID-1
	F
	E
3/6 Button	D
	C
Control PAD	B
	A
	9
	8
Adaptor	7
	6
Controller (Peripheral #1)	5
	4
Mouse	3
	2
	1
Modem	0

In detail, the CPU core 31 first determines whether or not the calculated result [ID-1] is Bh, for instance. When it is determined that the calculated result [ID-1] be Bh (YES at Step S106), it is decided that the peripheral device be a control PAD packed together with the game system. The relation between peripheral devices and

values of ID-1 is shown in Table 2. Thus the CPU core 31 performs the processing of a control PAD access subroutine (Step S111). When the calculated result [ID-1] is not Bh (NO at Step S106), the CPU core 31 then determines whether or not the calculated result [ID-1] is 5h, for example (Step S107).

When it is determined that the calculated result [ID-1] be 5h (YES at Step S107, also refer to Table 2), a controller access subroutine is processed (Step S112), which is shown in detail in Fig. 9.

When the calculated result [ID-1] is not 5h (NO at Step S107), the sub CPU 25 proceeds to the determination whether the calculated result [ID-1] is 7h, for example (Step S108). When the determination is YES at Step S108 (i.e., the calculated result [ID-1] = 7h), the sub CPU 25 then performs an adaptor access subroutine (Step S113).

When it is determined that the calculated result [ID-1] be not 7h (NO at Step S108), the sub CPU 25 continues to determine if the above calculated result [ID-1] is 3h or not, for example (Step S109). Where the calculated result [ID-1] is determined to be 3h (YES at Step S109, Table 2), a mouse access subroutine is processed (Step S114).

When the above result [ID-1] is not 3h (NO at Step S109), it is then determined whether or not the calculated result [ID-1] be Dh (Step S110). Where this determination shows that the calculated result [ID-1] is Dh (YES at Step S110, Table 2), a 3/6 button access subroutine is then performed (Step S115). When the determination

is NO at Step 110, the processing is continued to Step S116, where a decision that the peripheral device is not connected is made for the calculated result [ID-1] = Fh and a decision to be unknown is made for values of the [ID-1] other than the above exemplified results (refer to Table 2).

As a representative, the control PAD access subroutine will be described. In this subroutine, an access to the control PAD is carried out under the TH/TR-selection communication mode automatically designated. This communication mode uses 2-bit data consisting of combined two signals of the peripheral selection signal TH and data request signal TL to select a group of data generated in the control PAD. The selected group of data is supplied from the control PAD to the game apparatus. In the present embodiment, the TH/TR-selection communication mode is preferably employed in the control PAD and the 2-bit data can select four patterns for, for example, four-bit data R, L, D and U. The table 3 shows a truth values of this mode, in which the references "RIGHT", "LEFT", "DOWN", "UP", "START", and "TRG-A, B, C, X, Y, Z, L, R" are names of the key portions and switch portions. Data of the peripheral acknowledgment signal TL are ignored in the TH/TR-selection communication mode.

Table 3

DATA	TH	TR	TL	R	L	D	U
	bit6 INPUT	bit5 INPUT	bit4 OUT-PUT	bit3 OUT-PUT	bit2 OUT-PUT	bit1 OUT-PUT	bit0 OUT-PUT
1st	1	1	1	TRG-L	1	0	0
2nd	0	1	1	RIGHT	LEFT	DOWN	UP
3rd	1	0	1	STA-RT	TRG-A	TRG-C	TRG-B
4th	0	0	1	TRG-R	TRG-X	TRG-Y	TRG-Z

As another representative, the foregoing controller access subroutine shown in Fig. 9 will now be described also with reference to Table 4 which represents the bit patterns of data R, L, D and U corresponding to typical communication modes used by controllers as peripheral devices.

Table 4

Communication mode	TH=1 TR=1				TH=0 TR=1			
	R	L	D	U	R	L	D	U
Three-wire handshake	0	0	0	1	0	0	0	1
Clocked serial	0	0	1	0	0	0	1	0
Clocked parallel	0	0	1	1	0	0	1	1

In this access subroutine, the CPU core 31 of the sub CPU 25 first determines communication modes by a series of Steps S201 to S203 on the basis of the logical values of the data D and U acquired before. When both the data D is "0" and U is "1" (YES at Step S201), the peripheral device is identified as in the three-wire handshake mode (refer to Table 4), and the processing by the sub CPU 25 proceeds to a three-wire handshake-type access subroutine (Step S204).

When the data D and U are not "0" and "1", respectively (NO at Step S201), the CPU core 31 then determines whether both of the data D and U are "1" and "0", respectively, for example (Step S202). When the determination is YES at Step S202 (i.e., D="1" and U="0", refer to Table 3), the CPU core 31 continues to an access subroutine of the clocked serial communication mode (Step S205).

Furthermore, where the determination is NO at Step S202 (i.e., data D is not "1" and data U is not "0"), the CPU core 31 determines whether or not the data D is "1" and data U is "1" (Step S203). When

being determined that D="1" and U="1" (YES at Step S203, refer to Table 4), the CPU core 31 performs an access subroutine of the clocked parallel communication mode (Step S206).

When the CPU core cannot find the positive answers at any of the above determination processes at Steps S201 to S203 (NO at Steps S201 to S203), it is then determined that any peripheral device be not connected to the apparatus 2 (Step S207), and this subroutine is ended up.

Each access subroutine shown at the above Steps S204 to S206 will now be explained in detail.

First, the access subroutine of the three-wire handshake communication mode, which is shown in Fig. 10, will be explained using the timing chart of each signal shown in Fig. 13 in which the reference t shows time.

During the interval T_{11} in Fig. 13, the CPU core 31 reads the "peripheral ID-2" (Step S301 in Fig. 10). In other words, the data $ID\text{-}2_3$, $ID\text{-}2_2$, $ID\text{-}2_1$ and $ID\text{-}2_0$ of R, L, D and U are taken in by the CPU core 31 during the interval T_{11} and it is determined whether each of those data $ID\text{-}2_3$ to $ID\text{-}2_0$ corresponds to any of "0h" to "Fh" (refer to IDs shown in Table 5).

Table 5

Peripheral Device	ID-2	Remarks
Digital device	0	Control PAD, joystick etc.
Analog device	1	Analog joystick etc.
Pointing device	2	Mouse, tablet etc.
Keyboard	3	Keyboard etc.
Multitap	4	Multitap etc.
	5	
	6	
	7	
	8	
	9	
	A	
	B	
	C	
	D	
Peripheral #2	E	ID for conversion
	F	for non-connection

In addition to the reading, the CPU core 31 looks up Table 5 for each value of the read peripheral ID-2. For example, the CPU core 31 determines that the peripheral device be a digital device for "peripheral ID-2" = 0h, an analog device for "peripheral ID-2" = 1h, a

pointing device for "peripheral ID-2" = 2h, a key board for "peripheral ID-2" = 3h, and so on.

After such determination, the CPU core 31 reads the data size during the next interval T_{12} (Step S302). Namely, as shown in Fig. 13, data DSIZE0 to DSIZE3 of R, L, D and U are taken in for deciding the data size.

The CPU core 31 then reads the data during the following intervals starting from interval T_{13} in Fig. 12 (Step S303). It is then determined whether the amount of the read data reaches the data size (Step S304). If the determination is NO, the processing returns to Step S303 to read the data again. However, the determination is YES at Step S304 (i.e., the data amount that has been read by then reaches the determined data size), this subroutine is ended up.

Further, the access subroutine of the clocked parallel communication mode recited in Fig. 9 will now be explained using Figs. 11 and 14.

Fig. 14 shows the timing chart of the clocked parallel communication mode, which is almost the same as that shown in Fig. 13. Only one difference is that both of the signals TR and TL always change at the same timing, because of the short-circuit of pin nos. 5 and 6 in the plug connector 4ap (4bp).

First, the CPU core 31 reads the "peripheral ID-2" during the interval T_{21} in Fig. 14 (Step S401 in Fig. 11).

In detail, the data $ID\text{-}2_3$, $ID\text{-}2_2$, $ID\text{-}2_1$ and $ID\text{-}2_0$ of R, L, D and U are taken in by the CPU core 31 during the interval T_{21} and it is

determined whether each of the data ID-2_3 to ID-2_0 corresponds to any of "0h" to "Fh" (refer to IDs shown in Table 5). The CPU core 31 looks up Table 5 for each value of the read peripheral ID-2. For example, the CPU core 31 determines that the peripheral device be a digital device for "peripheral ID-2" = 0h, an analog device for "peripheral ID-2" = 1h, a pointing device for "peripheral ID-2" = 2h, a key board for "peripheral ID-2" = 3h, and so on.

After this, during the next interval T_{22}, the CPU core 31 reads the data size by receiving data DSIZE0 to DSIZE3 of R, L, D, U as shown in Fig. 14 (Step S402 in Fig. 11).

The CPU core 31 then reads the data during the following intervals starting from interval T_{23} in Fig. 14 (Step S403). It is then determined whether the amount of the read data reaches the data size (Step S404). If the determination is NO, the processing returns to Step S403 to read the data again. However, the determination is YES at Step S404 (i.e., the data amount that has been read by then reaches the determined data size), this subroutine is ended up.

Further, the access subroutine of the clocked serial communication mode will be explained according to Figs. 12 and 15 and Table 6. Fig. 15 exemplifies signal changes for the clocked serial mode, where the logical values of only the signals TH, TR and U are expressed along the elapsed time t.

This communication mode enables to obtain the data U only supplied from a peripheral device when the peripheral selection signal TH is "0" and at the same time, the data request signal TR is

repeatedly "1" and "0", both the signals TH and TR being given to the peripheral device from the CPU core 31. The obtained data are exemplified in Table 6.

Table 6

TH (input)	TR (input)	TL (GND)	R (GND)	L (GND)	D (Vcc)	U (DATA)	Remarks
1	1	0	0	0	1	0	ID-1(1st)
0	1	0	0	0	1	0	ID-2(2nd)
0	↓ ↑	0	0	0	1	SMD_3	
0	↓ ↑	0	0	0	1	SMD_2	
0	↓ ↑	0	0	0	1	SMD_1	
0	↓ ↑	0	0	0	1	SMD_0	
0	↓ ↑	0	0	0	1	$ID\text{-}2_3$	
0	↓ ↑	0	0	0	1	$ID\text{-}2_2$	
0	↓ ↑	0	0	0	1	$ID\text{-}2_1$	
0	↓ ↑	0	0	0	1	$ID\text{-}2_0$	
0	↓ ↑	0	0	0	1	$DSIZE_3$	
0	↓ ↑	0	0	0	1	$DSIZE_2$	
0	↓ ↑	0	0	0	1	$DSIZE_1$	
0	↓ ↑	0	0	0	1	$DSIZE_0$	
0	↓ ↑	0	0	0	1	$DATA_7$	
:	: :	:	:	:	:	:	
:	: :	:	:	:	:	:	
0	↓ ↑	0	0	0	1	$DATA_0$	

0	↓	↑	0	0	0	1	CCB	
0	↓	↑	0	0	0	1	1	
0	↓	↑	0	0	0	1	1	
0	↓	↑	0	0	0	1	0	
1	1		0	0	0	1	0	End M5ID-1st

As shown in Table 6, only when the peripheral selection signal TH is "0", the data request signal TR is repeated at cycles of "1" and "0" (expressed by upward and downward arrows in Table 6), the signal TL and data R and L are all "0", and the data D is "1", various data U including SMD_3 to SMD_0, $ID\text{-}2_3$ to $ID\text{-}2_0$, $DSIZE_3$ to $DSIZE_0$, and $DATA_7$ to $DATA_0$ are provided in sequence from the line U through the pin 3. Those data are read by the CPU core 31. Among them, the bit pattern of the data $ID\text{-}2_3$ to $ID\text{-}2_0$ are referred to the table 5 to decide the type of a connected peripheral device (Step S501 in Fig. 12).

The CPU core 31 reads the data size expressed by $DSIZE_0$ to $DSIZE_3$ (Step S502), so that the data size can be determined.

The data are then received by the CPU core 31 during predetermined intervals in a time sequence shown in Fig. 15 (Step S503). The amount of the read data are referred to the determined data size to determine whether the amount reaches the data size (Step S504). If the determination is NO, the processing returns to Step S503 to repeat the foregoing data read. The determination of YES at Step S504 allows to end up this subroutine.

As having been explained, the CPU core 31 exchanges signals with peripheral devices such that data "DATA" are inputted after information of "peripheral ID-1", "peripheral ID-2" and data size "DSIZE".

When the data are inputted into the CPU core 31, the CPU core 31 is to exchange data with the main CPU 21 through the register table 34.

In the above embodiment, although the sub CPU 25 controls the peripheral devices, the main CPU 21 can also perform the above-described processing instead of the sub CPU 25, if the main CPU 21 is directly connected to the peripheral devices.

Further, another identifying method of a communication mode can be used in the present invention. As is described above, the control signals TR and TL are equal in logical values (TR = TL) in the clocked parallel communication mode and the logical values on only specified pins (D, TL, R, L) are changed in specific manners. In case of the three-wire handshake mode, the control signals TR and TL are changed differently. This enables to calculate identification data of peripheral devices based on the pin configurations of the connectors and decide communication modes using the identification data.

Although the present invention has been described with reference to particular embodiments, the description is only an example of the invention's application and should not be taken as a limitation. In particular, the connector, the communication mode identifying system, and the peripheral device controlling system of

the present invention is not limited to use with the game apparatus and can also be applied to any other system which use a processing unit and at least one peripheral device thereof.

claimS

1. A peripheral device for use with a data processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins and being disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said ninth pin being assigned for connecting to the other of the power source and the ground potential, said second, third, seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins being assigned for transmitting control signals, said apparatus having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said second, third, seventh and eighth pins, said peripheral device comprising:

a plug connector which is to be detachably connected to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins and being disposed in row in the order of the first to the ninth pins correspondingly to said first to ninth pins of the peripheral port;

a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device; and

means for transmitting data signals including identification data representing the communication mode of said peripheral

device via at least one of said second, third, seventh and eighth pins in synchronization with a clock signal supplied from said apparatus when said plug connector is connected to said peripheral port.

2. The peripheral device of claim 1, wherein said fourth pins are assigned for transmitting a signal for activating the peripheral device, said fifth pins are assigned for transmitting the clock signal, wherein said peripheral device further comprises means for transmitting an acknowledgement signal to the apparatus via said sixth pins, and means for transmitting data signals to the apparatus via said second, third, seventh and eighth pins in synchronization with the clock signal.

3. The peripheral device of claim 1, wherein said fourth pins are assigned for transmitting a signal for activating the peripheral device, said fifth pins are assigned for transmitting the clock signal, wherein said peripheral device further comprises means for short-circuiting said sixth pin with said fifth pin, and means for transmitting parallel data signals to the apparatus via said third second, third, seventh and eighth pins in synchronization with the clock signal.

4. The peripheral device of claim 1, wherein said fourth pins are assigned for transmitting a signal for activating the peripheral device, said fifth pins are assigned for transmitting the clock

signal, wherein said peripheral device further comprises means for short-circuiting said second pin with said first pin, means for short-circuiting said sixth to eighth pins with said ninth pin, means for transmitting serial data signals to the apparatus via said third pin in synchronization with the clock signal.

5. A peripheral device for use with a data processing apparatus having a peripheral port to which a plug connector of said peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is to be detachably connected to said peripheral port, said plug connector having a set of terminal pins including first to ninth pins and being disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said ninth pin being assigned for connecting to the other of the power source and the ground potential, said second, third, seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins being assigned for transmitting control signals;

a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device; and

means for transmitting data signals including identification data representing the communication mode of said peripheral device to the apparatus via at least one of said second, third,

seventh and eighth pins in synchronization with a clock signal supplied from said apparatus when said plug connector is connected to said peripheral port.

6. A peripheral device for use with a data processing apparatus having a socket connector with a set of socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is to be detachably connected to the socket connector, said plug connector having a set of plug pins disposed in a row and correspondingly to the socket pins, said plug pins including a pair of first pins assigned for connecting to fixed potentials, at least one second pin assigned for transmitting data signals, and third pins assigned for transmitting control signals;

mean for configuring said set of plug pins so that the configuring arrangement is indicative of the communication mode of the peripheral device;

a cable including a plurality of wires connecting the plug pins with terminals on a printed circuit board of said peripheral device; and

means for transmitting data signals including identification data representing the communication mode of said peripheral device via said at least one second pin in synchronization with a clock signal supplied via one of said third pins from said apparatus when said plug connector is connected to said peripheral port.

7. The peripheral device of claim 6, wherein said configuring means includes means for short-circuiting specified pins.

8. A peripheral device for use with a data processing apparatus having a socket connector with nine of socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is to be detachably connected to said socket connector, said plug connector having nine of plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins assigned for connecting to fixed potentials, four of second pins assigned for transmitting data signals, and three of third pins assigned for transmitting control signals;

a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device;

means for short-circuiting two of said third pins with one another; and

means for transmitting parallel data signals including identification data representing the communication mode of said peripheral device via said second pins in synchronization with a clock signal supplied via one of said third pins from said apparatus when said plug connector is connected to said peripheral port.

9. The peripheral device of claim 8, wherein said short-circuiting

means is formed on said plug connector.

10. The peripheral device of claim 9, wherein the wires of said cable are less in number than said socket pins.

11. A peripheral device for use with a data processing apparatus having a socket connector with nine of socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is to be detachably connected to said socket connector, said plug connector having nine of plug pins disposed correspondingly to the socket pins, said plug pins including a pair of first pins assigned for connecting to fixed potentials, a second pin assigned for transmitting data signals, and two of third pins assigned for transmitting control signals;

a cable including a plurality of wires connecting the terminal pins of said plug connector with terminals on a printed circuit board of said peripheral device;

means for short-circuiting the remaining pins other than said first to third pins to at least one of said first pins; and

means for transmitting serial data signals including identification data representing the communication mode of said peripheral device via said second pin in synchronization with a clock signal supplied via one of said third pins from said apparatus when said plug connector is connected to said peripheral port.

12. The peripheral device of claim 11, wherein said short-circuiting means are formed in said plug connector.

13. The peripheral device of claim 11, wherein the wires in said cable are less in number than said socket pins.

14. In combination of a data processing apparatus and a peripheral device, comprising:

said apparatus having a peripheral port with a plurality of terminal pins disposed in a row, said terminal pins including a pair of first pins, one assigned for connecting to one of a power source and the ground potential and the other assigned for connecting to the other of the power source and the ground potential, at least one of second pins assigned for transmitting data signals, a plurality of third pins assigned for transmitting control signals, said apparatus further having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said at least one second pin, means for transmitting a clock signal via one of said third pins to said peripheral device and means for performing a communication with the connected peripheral device with the selected communication mode;

said peripheral device having a plug connector which is to be detachably connected to said peripheral port, said plug connector having a plurality of terminal pins configured as the same in number as and disposed in a row correspondingly to the terminal

pins of said peripheral port, said peripheral device further having a cable including a plurality of wires connecting the terminal pins of said plug connector with terminal on a printed circuit board of said peripheral device and means for transmitting data signals including identification data representing the communication mode of said peripheral device via said at least one of second pin to said apparatus in synchronization with said clock signal when said plug connector is connected to said peripheral port.

15. The invention of claim 14, wherein said peripheral port comprises four of the second pins and three of the third pins, said second and third pins being disposed in positions of the row between said pair of first pins.

16. The invention of claim 15, wherein said plug connector comprises a pair of first pins, four of the second pins and three of the third pins, each being disposed correspondingly to those in said peripheral port.

17. The invention of claim 16, wherein said apparatus further comprising means for transmitting a signal for activating said peripheral device via one of said third pins in the peripheral port different from the one for transmitting the clock signal, said peripheral device further comprises means for transmitting an acknowledging signal to the apparatus via the remaining one of said third pins in said peripheral port, and the data signals are

transmitted via said four of the second pins.

18. The invention of claim 16, wherein said apparatus further comprising means for transmitting a signal for activating said peripheral device via one of said third pins in the peripheral port different from the one for transmitting the clock signal, said peripheral device further comprises means for short-circuiting two of the third pins other than one through which the activating signal is transmitted, and means for transmitting parallel data signals via said four of the second pins.

19. The invention of claim 16, wherein said apparatus further comprising means for transmitting a signal for activating said peripheral device via one of said third pins in the peripheral port different from the one for transmitting the clock signal, said peripheral device further comprises means for transmitting serial data signals via one of the second pins to said apparatus, and means for short-circuiting the remaining one of the third pins and the remaining three of the second pins with the said first pins.

20. In combination of a data processing apparatus and a peripheral device, comprising:

said apparatus having a socket connector with a set of socket pins consisting of first to ninth pins disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said

ninth pin being assigned for connecting to the other of the power source and the ground potential, said second, third, seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins assigned for transmitting control signals,

said apparatus further comprising first means for supplying to said fourth pin a signal for activating said peripheral device, second means for reading data signals produced at said second, third, seventh and eighth pins, third means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals read by said second means, fourth means for transmitting a clock signal to said fifth pin, and fifth means for performing a communication with the connected peripheral device with the selected communication mode;

said peripheral device having a plug connector which is to be detachably connected to said socket connector, said plug connector having a set of plug pins consisting of first to ninth pins configured as the same in number as, and disposed in a row in the order of the first to the ninth pins correspondingly with said socket pins,

said peripheral device further comprising a cable including a plurality of wires connecting the plug pins with terminals on a printed circuit board of said peripheral device and sixth means for transmitting data signals including identification data representing the communication mode of said peripheral device via at least one of said second, third, seventh and eighth plug pins to said apparatus in synchronization with said clock signal when said

plug connector is connected to said socket connector.

21. The invention of claim 20, wherein said peripheral device further comprises seventh means for transmitting an acknowledge signal to the apparatus via the sixth plug pin, and the data signals are transmitted via said second, third, seventh and eighth plug pins.

22. The invention of claim 20, wherein said peripheral device further comprises seventh means for short-circuiting the sixth plug pin with fifth plug pin, and eighth means for transmitting parallel data signals via said second, third, seventh and eighth plug pins.

23. The invention of claim 20, wherein said peripheral device further comprises seventh means for transmitting serial data signals via the third plug pin, eighth means for short-circuiting the second plug pin with the first plug pin, and ninth means for short-circuiting the sixth to eighth plug pins with the ninth plug pin.

24. A peripheral device for use with an information processing apparatus, said apparatus having a peripheral port with a set of terminal pins consisting of first to ninth pins and being disposed in a row in the order of the first to the ninth pins, said first pin being assigned for connecting to one of a power source and the ground potential, said ninth pin being assigned for connecting to the other of the power source and the ground potential, said second, third,

seventh and eighth pins being assigned for transmitting data signals, said fourth to sixth pins being assigned for transmitting control signals, said apparatus having means for selecting the communication mode for communicating with the peripheral device connected to the peripheral port based on the data signals transmitted from said second, third, seventh and eighth pins, said peripheral device comprising:

a plug connector which is to be detachably connected to said peripheral port, said plug connector having a set of terminal pins consisting of first to ninth pins and being disposed in row in the order of the first to the ninth pins correspondingly to said first to ninth pins of the peripheral port; and

means for transmitting data signals including identification data representing the communication mode of said peripheral device via at least one of said second, third, seventh and eighth pins in synchronization with a clock signal supplied from said apparatus when said plug connector is connected to said peripheral port.

25. A peripheral device for use with an information processing apparatus having a socket connector with a set of socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is to be detachably connected to the socket connector, said plug connector having a set of plug pins disposed in a row and correspondingly to the socket pins, said plug

pins including a pair of first pins assigned for connecting to fixed potentials, at least one second pin assigned for transmitting data signals, and third pins assigned for transmitting control signals, said set of plug pins being configured so that the configuring arrangement is representative of the communication mode of the peripheral device; and

means for transmitting data signals including identification data representing the communication mode of said peripheral device via said at least one second pin in synchronization with a clock signal supplied via one of said third pins from said apparatus when said plug connector is connected to said peripheral port.

26. A peripheral device for a game apparatus having a socket connector with a set of nine (9) socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is detachably connected to the socket connector, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins and correspondingly to said socket pins, the first pin being assigned to a power source potential, the ninth pin being assigned to the ground potential, the sixth pin being assigned for transmitting control signals from the peripheral device to the game apparatus, and

means for transmitting to the game apparatus data signals representing a three-wire handshake type communication mode, including means, when a control signal of "1" to the fourth pin and

"1" to the fifth pin and a control signal of "0" to the fourth pin and "1" to the fifth pin are supplied from the game apparatus, for supplying a data signal of "0" to the seventh pin, "0" to the eighth pin, "0" to the second pin and "1" to the third pin, respectively, wherein "1" stands for the power source potential and "0" stands for the ground potential, whereby the game apparatus determines that the peripheral device connected to the socket connector is of the three-wire handshake type communication mode.

27. A peripheral device for a game apparatus having a socket connector with a set of nine (9) socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is detachably connected to the socket connector, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins and correspondingly to said socket pins, the first pin being assigned to a power source potential, the second pin being assigned to the ground potential, the sixth pin being assigned for transmitting control signals from the peripheral device to the game apparatus, and

means for transmitting to the game apparatus data signals representing a clocked parallel type communication mode, including means for connecting the fifth pin with the sixth pin and means, when a control signal of "1" to the fourth pin and "1" to the fifth pin and a control signal of "0" to the fourth pin and "1" to the fifth pin are supplied from the game apparatus, for supplying a data sinal of

"0" to the seventh pin, "0" to the eighth pin, "1" to the second pin and "1" to the third pin, respectively, wherein "1" stands for the power source potential and "0" stands for the ground potential, whereby the game apparatus determines that the peripheral device connected to the socket connector is of the clocked parallel type communication mode.

28. A peripheral device for a game apparatus having a socket connector with a set of nine (9) socket pins to which a plug connector of the peripheral device is detachably connected, said peripheral device comprising:

a plug connector which is detachably connected to the socket connector, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins and correspondingly to said socket pins, the first pin being assigned to a power source potential, the ninth pin being assigned to the ground potential, and

means for transmitting to the game apparatus data signals representing a clocked serial type communication mode, including means for connecting the second pin with the first pin, means for connecting the sixth, the seventh and the eighth pins with ninth pin, and means, when a control signal of "1" to the fourth pin and "1" to the fifth pin and a control signal of "0" to the fourth pin and "1" to the fifth pin are supplied from the game apparatus, for supplying a data signal of "0" to the seventh pin, "0" to the eighth pin, "1" to the second pin and "0" to the third pin, respectively, wherein "1" stands for the power source potential and "0" stands for the ground

potential, whereby the game apparatus determines that the peripheral device connected to the socket connector is of the clocked serial type communication mode.

29. A peripheral device for a game apparatus having a connector port to which a plug connector of the peripheral device is detachably connected, comprising:

a plug connector which is detachably connected to the socket port, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins, the first pin being supplied with a power source, the ninth pin being supply with the ground potential, and

means for transmitting to the game apparatus data signals indicative of a three-wire handshake type communication mode, including means for supplying a data signal of "0" to the second pin and "1" to the third pin in response to a control signal from the game apparatus wherein "1" sands for the power source potential and "0" stands for the ground potential, whereby the game apparatus determines that the peripheral device connected to the connector port is of the three-wire handshake type communication mode.

30. A peripheral device for a game apparatus having a connector port to which a plug connector of the peripheral device is detachably connected, comprising:

a plug connector which is detachably connected to the socket

port, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins, the first pin being supplied with a power source, the ninth pin being supplied with the ground potential, and

means for transmitting to the game apparatus data signals indicative of a clocked parallel type communication mode, including means for connecting the fifth pin with the sixth pin and means for supplying a data signal of "1" to the second pin and "1" to the third pin in response to a control signal from the game apparatus wherein "1" stands for the power source potential and "0" stands for the ground potential, whereby the game apparatus determines that the peripheral device connected to the connector port is of the clocked parallel type communication mode.

31. A peripheral device for a game apparatus having a connector port to which a plug connector of the peripheral device is detachably connected, comprising:

a plug connector which is detachably connected to the socket port, said plug connector having a set of nine (9) plug pins disposed in a row from the first to ninth pins, the first pin being supplied with a power source, the ninth pin being supplied with the ground potential, and

means for transmitting to the game apparatus data signals indicative of a clocked serial type communication mode, including means for connecting the second pin with the first pin, means for connecting the sixth, the seventh and the eighth pins with the ninth

pin, and means for supplying a data signal of "1" to the second pin and "0" to the third pin in response to a control signal from the game apparatus, wherein "1" stands for the power source potential and "0" stands for the ground potential, whereby the game apparatus determines that the peripheral device connected to the connector port is of the clocked serial type communication mode.

32. A peripheral device for a game apparatus used by being connected to a socket connector of said game apparatus, said peripheral device having a plug connector to be detachably connected to said socket connector, said plug connector having nine (9) connector pins disposed in a row corresponding to said socket connector, said connector pins including a first pin, a second pin, a third pin, a fourth pin, a fifth pin, a seventh pin, an eighth pin, and a ninth pin, the first pin being supplied with a power source potential and the ninth pin being supplied with a ground potential from said game apparatus, said plug connector for supplying said game apparatus with data from said peripheral device via the seventh pin, the eighth pin, the second pin and the third pin when, under the condition that "1" stands for the power source potential and "0" stands for the ground potential, said peripheral device being supplied with control signals from said game apparatus alternatively in a first mode or a second mode, such that in the first mode the fourth pin becomes "1" and the fifth pin becomes "1," and such that in the second mode the fourth pin becomes "0" and the fifth pin becomes "1," wherein when the control signals are in

the first mode or in the second mode then the game apparatus determines a peripheral ID based upon the data from the seventh pin, the eighth pin, the second pin, and the third pin, and the game apparatus determines that a selection mode between the peripheral device and the game adaptor is a TH/TR-selection communication mode.

33. A peripheral device for a game apparatus according to Claim 32, said peripheral device comprising a standard control pad with a plurality of keys disposed thereon to be manually operated by a player.

34. A peripheral device for a game apparatus according to Claim 33, said peripheral device constructed such that when said game apparatus supplies said control pad with control signals to make the fourth pin "1" and the fifth pin "1," the control pad transmits data back to said game apparatus making the seventh pin a "signal assigned to one key, " the eighth pin "1," the second pin "0," and the third pin "0," and when said game apparatus supplies said control pad with control signals to make the fourth pin "0" and the fifth pin "1," the control pad transmits data back to said game apparats to make the seventh pin, the eighth pin, the second pin, and the third pin each a different "signal assigned to one key."

35. A peripheral device for a game apparatus according to Claim 33, said peripheral device constructed such that, when said two

data select signals are supplied to said control pad via said fourth and fifth pins from said game apparatus, the control pad prepares said signals for a plurality of keys pre-classified in four groups as 4-bit data for each group in correspondence with the combination of bits of such two data select signals, and the control pad transmits such prepared 4-bit data back to said game apparatus via said seventh pin, eighth pin, second pin and third pin.

36. A peripheral device for a game apparatus according to Claim 34, said peripheral device constructed such that, when said two data select signals are supplied to said control pad via said fourth and fifth pins from said game apparatus, the control pad prepares said signals for a plurality of keys pre-classified in four groups as 4-bit data for each group in correspondence with the combination of bits of such two data select signals, and the control pad transmits such prepared 4-bit data back to said game apparatus via said seventh pin, eighth pin, second pin and third pin.

37. A connector for connecting a peripheral device to a processing apparatus having a socket connector incorporating nine terminal pins therein, said connector comprising a plug connector being detachably connected to the socket connector and incorporating nine terminal pins disposed in a row in the order of the first to ninth pins each contacting with each of the nine terminal pins of the socket connector, a power source and a ground potential being supplied respectively to the first and ninth pins of the terminal

pins from the processing apparatus, control signals being supplied through the fourth and fifth pins of the plug connector from the processing apparatus to the peripheral device, and data signals in accordance with a communication mode of the peripheral device being supplied through at least one of the second, third, seventh and eighth pins from the peripheral device to the processing apparatus.

38. The connector of claim 37, wherein said peripheral device is a peripheral device supplying to the processing apparatus another control signal through the sixth pin of the terminal pins of the plug connector and the data signals in accordance with a three-wire handshake communication mode through the second, third, seventh, and eighth pins of the terminal pins of the plug connector.

39. The connector of claim 37, wherein said sixth pin is short-circuited with said fifth pin in the terminal pins of the plug connector and said peripheral device is a peripheral device supplying to the processing apparatus the data signals in accordance with a clocked parallel communication mode through the second, third, seventh, and eighth pins of the terminal pins of the plug connector.

40. The connector of claim 37, wherein said second pin is short-circuited with said first pin and said sixth to eighth pins are short-circuited with said ninth pin and said peripheral device is a peripheral device supplying to the processing apparatus the data

signal in accordance with a clocked serial communication mode through the third pin of the terminal pins of the plug connector.

41. The connector of claim 37, wherein said peripheral device is a peripheral device requiring a data selecting signal of two bits supplied through said fourth and fifth pins of the terminal pins of the plug connector from the processing apparatus.

42. A connector for connecting a peripheral device having a clocked serial communication mode to a processing apparatus, comprising a plug connector detachably connected to a socket connector of the processing apparatus, said plug connector having nine terminal pins disposed in an array in the order of the first to ninth pins each contacting with nine pins of the socket connector, said first and ninth pins receiving a power source and a ground potential respectively, said second pin being short-circuited with said first pin, said sixth to eighth pins being short-circuited with said ninth pin, a single first cable being connected from either one of said first and second pins, a single second cable being connected from one of said sixth to ninth pins, and single third to fifth cables being connected from said third to fifth pins respectively,

wherein control signals are transmitted through said fourth and fifth pins, and data in accordance with the clocked serial communication mode are transmitted from the peripheral device to the processing apparatus.

AMENDED CLAIMS

[received by the International Bureau on 9 April 1996 (09.04.96); original claims 1-42 replaced by amended claims 1-33 (11 pages)]

1. A peripheral device for use with a data processing apparatus, comprising a plug connector detachably connectable to a peripheral port formed on the data processing apparatus, and means for transmitting data signals to the data processing apparatus through the plug connector, characterized in:

that the plug connector comprises a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to a set of terminal pins disposed at the peripheral port, the first pin for supplying one of a power source and a ground potential, the ninth pin for supplying the other of the power source and the ground potential, the second, third, seventh and eighth pins for conducting data signals, and the fourth to sixth pins for conducting control signals;

that the data signals includes identification data representing a communication mode of the peripheral device and are supplied to the apparatus via at least one of the second, third, seventh and eighth pins by a data request signal supplied from the apparatus; and

that the apparatus determines the communication mode for communicating with the peripheral device based on the data signals received on the second, third, seventh and eighth pins of the peripheral port.

2. The peripheral device of claim 1, characterized in that the fourth and fifth pins of the apparatus are for transmitting a signal for activating the peripheral device and for transmitting the data request signal, respectively, and that the peripheral device further comprises means for transmitting an acknowledgement signal to the apparatus via the sixth pin of the plug connector and means for transmitting data signals to the apparatus via the second, third, seventh and eighth pins of the plug connector in synchronism with the clock signal.

3. The peripheral device of claim 1, characterized in that the fourth and fifth pins of the apparatus are for transmitting a signal for activating the peripheral device and for transmitting the clock signal as said data request signal, respectively, and that the peripheral device further comprises means for maintaining the sixth pin at the same potential as on the fifth pin and means for transmitting parallel data signals to the apparatus via the second, third, seventh and eighth pins of the plug connector in synchronism with the clock signals.

4. The peripheral device of claim 1, characterized in that the fourth and fifth pins of the apparatus are for transmitting a signal for activating the peripheral device and for transmitting the clock signal, respectively; and

that the peripheral device further comprises first means for maintaining the second pin at the same potential as on the

first pin, second means for maintaining the sixth, seventh and eighth pins at the same potential as on the ninth pin, and means for transmitting serial data signals to the apparatus via the third pin in synchronism with the clock signals.

5. A peripheral device for use with a data processing apparatus, comprising a plug connector detachably connectable to a socket connector formed at a peripheral port on the apparatus, and means for transmitting data signals to the apparatus via the plug connector, characterized in that the plug connector comprises a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to a set of terminal pins disposed in the socket connector, the first pin for receiving a power source potential, the ninth pin for receiving a ground potential, the second, third, seventh and eighth pins for conducting data signals, and the fourth to sixth pins for conducting control signals;

that the peripheral device supplies the apparatus with a data signal representing a communication mode of the peripheral device via at least one of the second, third, seventh and eighth pins when a control signal of "1" to the fourth pin and "1" to the fifth pin or a control signal of "0" to the fourth pin and "1" to the fifth pin are supplied from the apparatus wherein "1" and "0" correspond to the power source and ground potentials, respectively; and

that the apparatus determines the communication mode for communicating with the peripheral device based on the data

signals received on the second, third, seventh and eighth pins of the peripheral port.

6. The peripheral device according to claim 5, characterized in that the peripheral device supplies a signal of "0" to the seventh pin, "0" to the eight h pin, "0" to the second pin and "1" to the third pin, respectively, when the peripheral device is supplied with the control signals whereby the apparatus determines that the peripheral device connected to the socket connector employs the three-wire hand-shake type communication mode.

7. The peripheral device according to claim 5, characterized in that the peripheral device comprises means for maintaining the sixth pin at the same potential as on the fifth pin and that the peripheral device supplies a signal of "0" to the seventh pin, "0" to the eighth pin, "1" to the second pin and "1" to the third pin, respectively, when the peripheral device is supplied with the control signals whereby the apparatus determines that the peripheral device connected to the socket connector employs the clocked parallel type communication mode.

8. The peripheral device according to claim 5, characterized in that the peripheral device supplies a signal of "0" to the seventh pin, "0" to the eighth pin, "1" to the second pin and "0" to the third pin, respectively, when the peripheral device is supplied with the control signals, whereby the apparatus

determines that the peripheral device connected to the socket connector employs the clocked serial type communication mode.

9. A peripheral device for use with a data processing apparatus, comprising a plug connector detachably connectable to a socket connector formed at a peripheral port on the apparatus, means for transmitting data signals to the apparatus through the plug connector, characterized in that the plug connector comprises a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to a set of terminal pins disposed in the socket connect, the first pin for receiving a power source, the ninth pin for receiving a ground potential, the second, third, seventh and eighth pins for conducting data signals, and the fourth to sixth pins for conducting control signals;

that the peripheral device is supplied with control signals from the apparatus alternatively in a first signal combination in which the fourth pin becomes "1" and the fifth pin becomes "1", or in a second signal combination in which the fourth pin becomes "0" and the fifth pin becomes "1", wherein "1" and "0" correspond to the power source and ground potentials, respectively; and

that, when the control signals are in the first or second signal combination, the apparatus determines a peripheral ID based upon the data from the second, third, seventh and eighth pins, and then determines that the peripheral device connected to the socket connector employs a TH/TR communication mode.

peripheral device comprises a plurality of switching keys disposed thereon to be manually operated by a player.

11. The peripheral device according to claim 10, characterized in that the apparatus supplies data select signals TH and TR to the peripheral device via the fourth and fifth pins, respectively; and

that the peripheral device transmits various sets of data signals responsive to the data select signals TH and TR via the seventh, eighth, second and third pins, the various sets of data signals including data indicative of status of the switching keys.

12. The peripheral device according to claim 11, characterized in that, when the data select signals TH and TR are "1" and "1", respectively, the peripheral device transmits data back to the apparatus assigning the seventh pin as a signal path to one of the switching keys, the eighth pin "1", the second pin "0", and the third pin "0"; and

that, when the data select signals TH and TR are "0" and "1", or "1" and "0", or "0" and "0", the peripheral device supplying the apparatus with data indicative of status of the switching keys via the seventh, eighth, second and third pins, respectively.

13. The peripheral device according to claim 12, characterized in that the sixth pin is supplied with "1" all the time while the data select signals are supplied.

that the means for maintaining includes means for short-circuiting the sixth pin with the fifth pin.

15. The peripheral device of claim 4, characterized in that the first means for maintaining includes means for short-circuiting the second pin with the first pin and the second means for maintaining includes means for short-circuiting the sixth, seventh and eighth pins with the ninth pin.

16. The peripheral device of any one of claims 1 to 8, characterized in that the peripheral device further comprises means for configuring the set of the terminal pins of the plug connector to be indicative of the communication mode of the peripheral device.

17. The peripheral device of claim 16, characterized in that said configuration means includes means for short-circuiting selected ones of the terminal pins of said plug connector.

18. The peripheral device of any one of the preceding claim, characterized in further comprising a printed circuit board on which means for generating the data signals to be supplied to the apparatus is formed, and a cable including a plurality of wires connecting the terminal pins of the plug connector with the printed circuit board.

17, characterized in that the short-circuiting means are formed in the plug connector.

20. The peripheral device of claim 18, characterized in that the wires of the cable are fewer in number than the pins on the peripheral port.

21. The peripheral device of claim 18, characterized in that the plug connector comprises means for short-circuiting selected ones of pins, and the wires of the cable are fewer in number than the pins on the peripheral port.

22. The peripheral device of any one of claims 14, 15 and 17, characterized in that the short-circuiting means are formed on the circuit board.

23. A game apparatus comprising the data processing apparatus and the peripheral device as defined in any one of the preceding claims.

24. A device connector for connecting the peripheral device to the data processing apparatus as defined in any one of the preceding claims, further characterized in that the pins are formed with elongated contacts disposed parallely in a row.

25. A device connector for connecting a peripheral device to a data processing apparatus having a socket connector with nine terminal pins, characterized in that the device connector comprises a plug connector detachably connectable to the

terminal pins disposed correspondingly to the nine terminal pins of the socket connector, the terminal pins of the plug connector being formed with elongated contacts disposed parallely in a row;

that the first and ninth terminal pins of the plug connector are respectively for connecting to a power source and ground potential supplied from the apparatus; and

that at least one of the second, third, seventh and eighth terminal pins of the plug connector is for conducting data signals supplied from the peripheral device which represent a communication mode of the peripheral device.

26. The device connector of claim 25, characterized in that the sixth pin is for conducting a control signal supplied from the peripheral device, and the second, third, seventh and eighth terminal pins are for conducting the data signals from the peripheral device in a three-wire handshake communication mode.

27. The device connector of claim 25, characterized in that the fifth and sixth terminal pins of the plug connector are short-circuited together and the second, third, seventh and eighth terminal pins of the plug connector are for conducting the data signals supplied from the peripheral device in a clocked parallel communication mode.

28. The device connector of claim 25, characterized in that the first and second terminal pins of the plug connector are short-circuited together, the sixth through eighth terminal

the third terminal pin of the plug connector is for conducting the data signals supplied from the peripheral device in a clocked serial communication mode.

29. The device connector of claim 25, characterized in that the fourth and fifth terminal pins are for conducting 2 bit data selecting signals supplied to the peripheral device from the processing apparatus.

30. A peripheral device for use with a data processing apparatus, comprising a plug connector detachably connectable to a peripheral port formed on the data processing apparatus, and means for transmitting a data signals to the data processing apparatus through the plug connector, characterized in that the plug connector comprises a set of terminal pins consisting of first to ninth pins disposed in a row correspondingly to a set of terminal pins disposed at the peripheral port;

that the terminal pins of the plug connector are predeterminedly configured in accordance with a communication mode between the processing apparatus and the peripheral device;

that the data signals include identification data representing a communication mode of the peripheral device and are supplied to the apparatus via at least one of the terminal pins in synchronism with clock signals supplied from the data processing apparatus; and

that the data processing apparatus determines the communication mode for communicating with the peripheral

said other terminal pins.

31. A device connector for connecting a peripheral device to a data processing apparatus having a socket connector with nine terminal pins, characterized in:

that the device connector comprises a plug connector detachably connectable to the socket connector, the plug connector has first to ninth terminal pins disposed correspondingly to the nine terminal pins of the socket connector, the terminal pins of the plug connector and socket connector are formed with elongated contacts disposed in parallel, in a row;

that the terminal pins of the plug connector are predeterminedly configured in accordance with a communication mode of the peripheral; and

at least one of terminal pins of the plug connector is for conducting data signals supplied from the peripheral device which represent a communication mode of the peripheral device.

32. The peripheral device of any one of claims 1-8, characterized in that the peripheral device comprises a plurality of switching keys disposed thereon to be manually operated by a player.

33. The devise connector of claim 25, characterized in that a control signal is supplied through the fourth and fifth pins of the plug connector from the processing apparatus to the peripheral device.

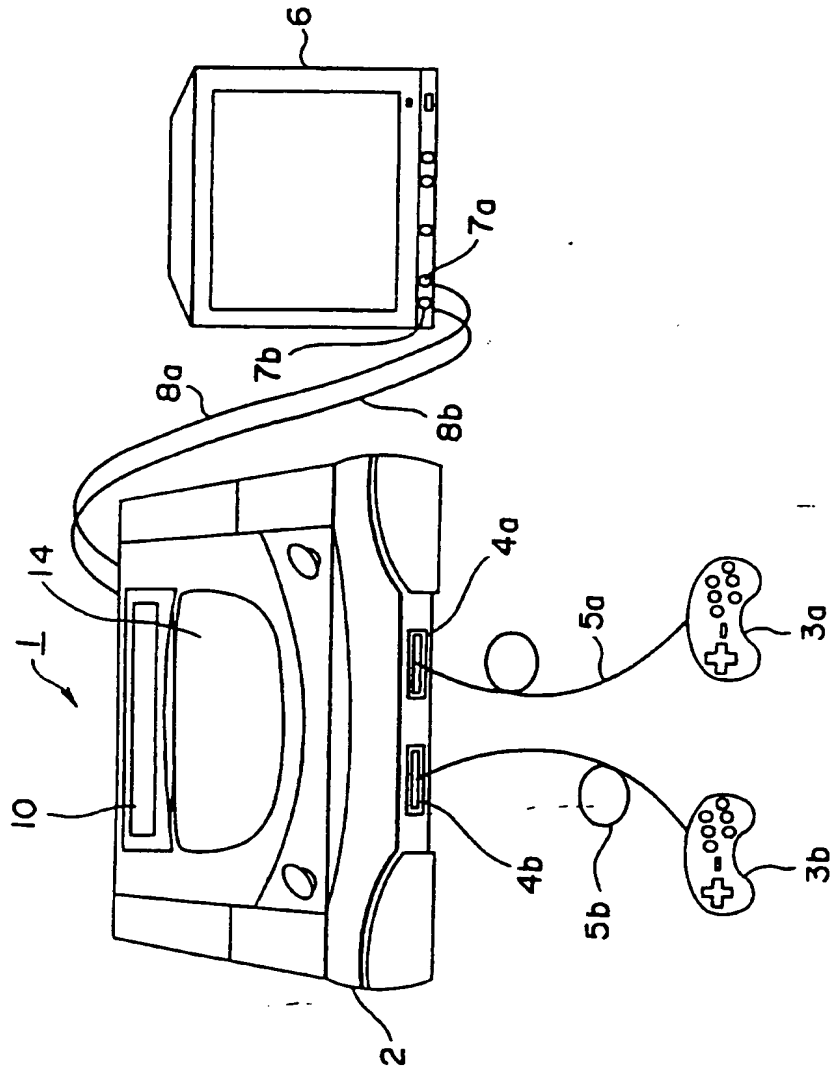


FIG.1

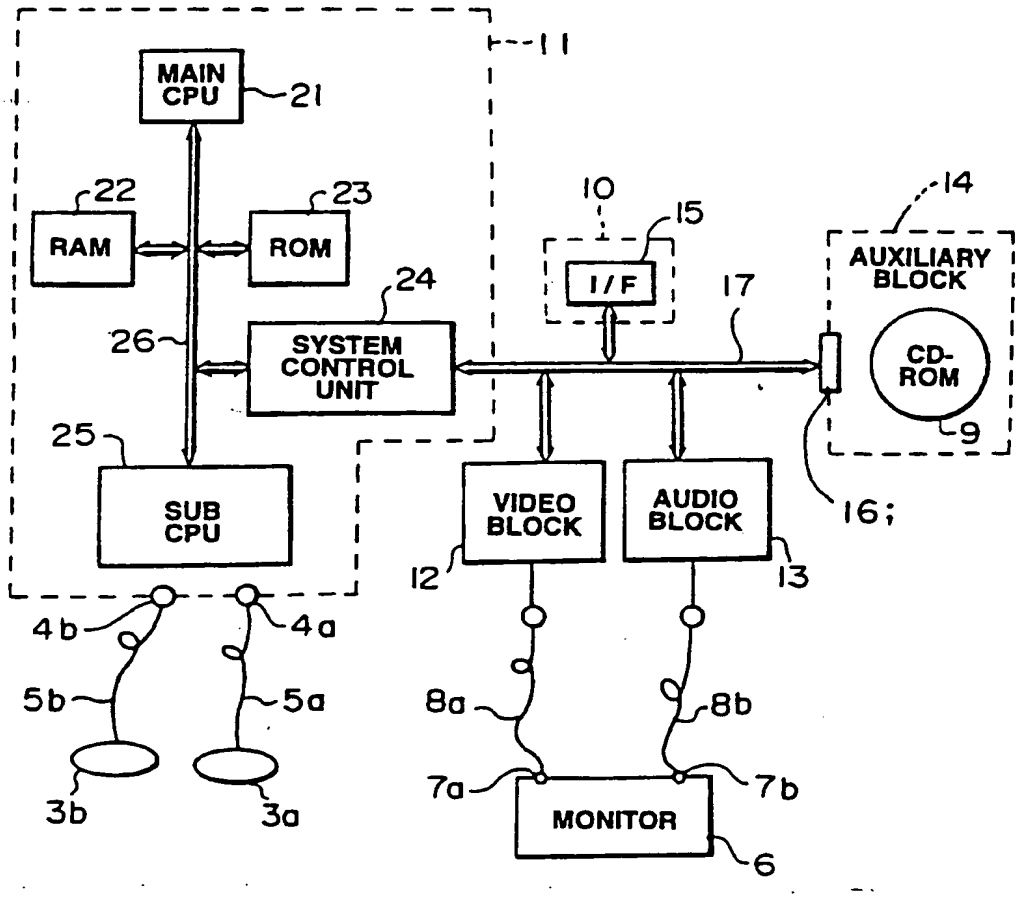

11
MAIN CPU
21
22
RAM
23
ROM
24
26
SYSTEM CONTROL UNIT
25
SUB CPU
10
15
I/F
17
14
AUXILIARY BLOCK
CD-ROM
9
16
VIDEO BLOCK
12
AUDIO BLOCK
13
4b
4a
5b
5a
3b
3a
8a
8b
7a
7b
MONITOR
6

FIG.2

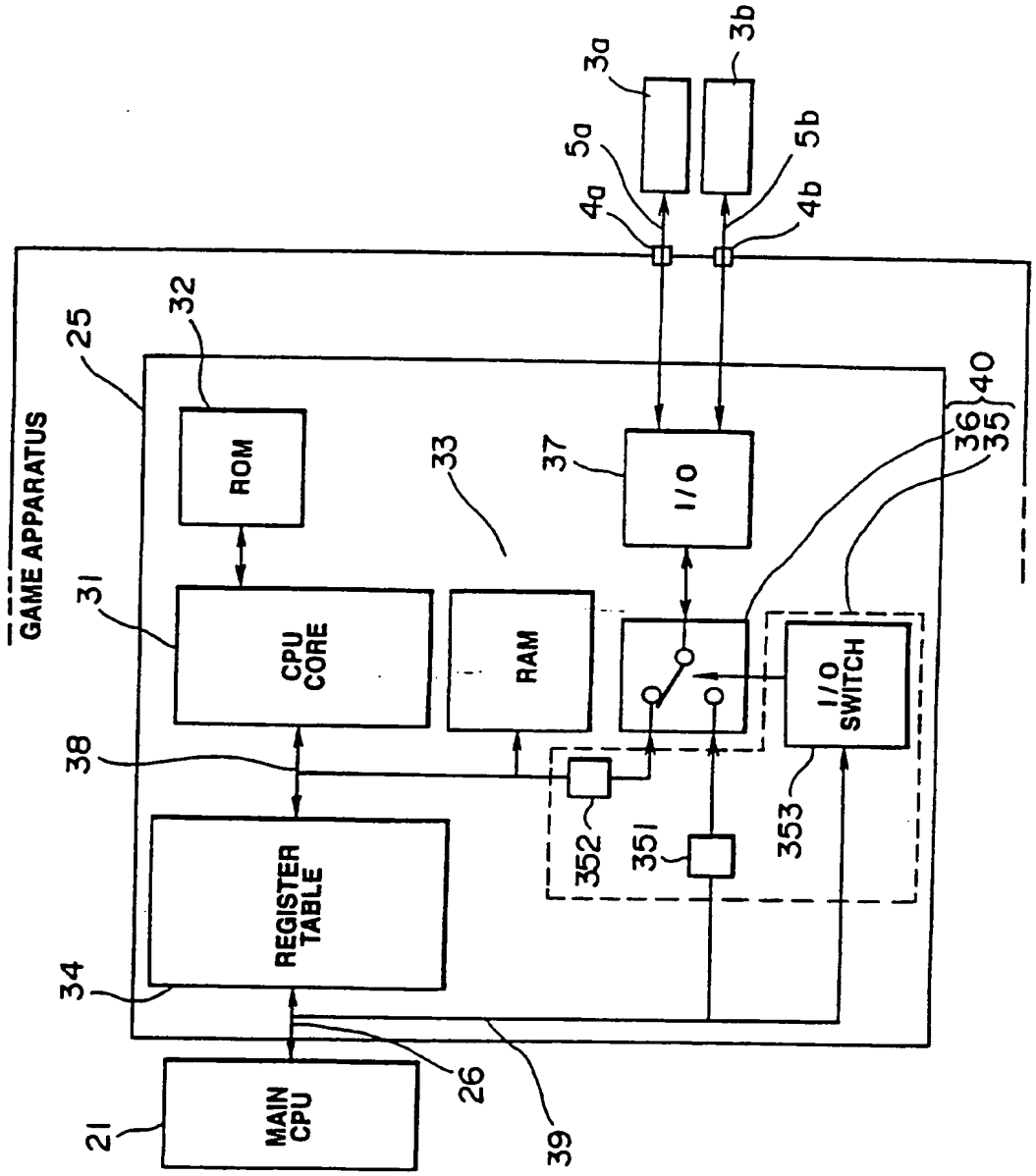

GAME APPARATUS
25
32
ROM
31
CPU CORE
33
RAM
37
I/O
36
35
40
I/O SWITCH
38
352
351
353
REGISTER TABLE
34
MAIN CPU
21
26
39
3a
3b
5a
5b
4a
4b

FIG.3

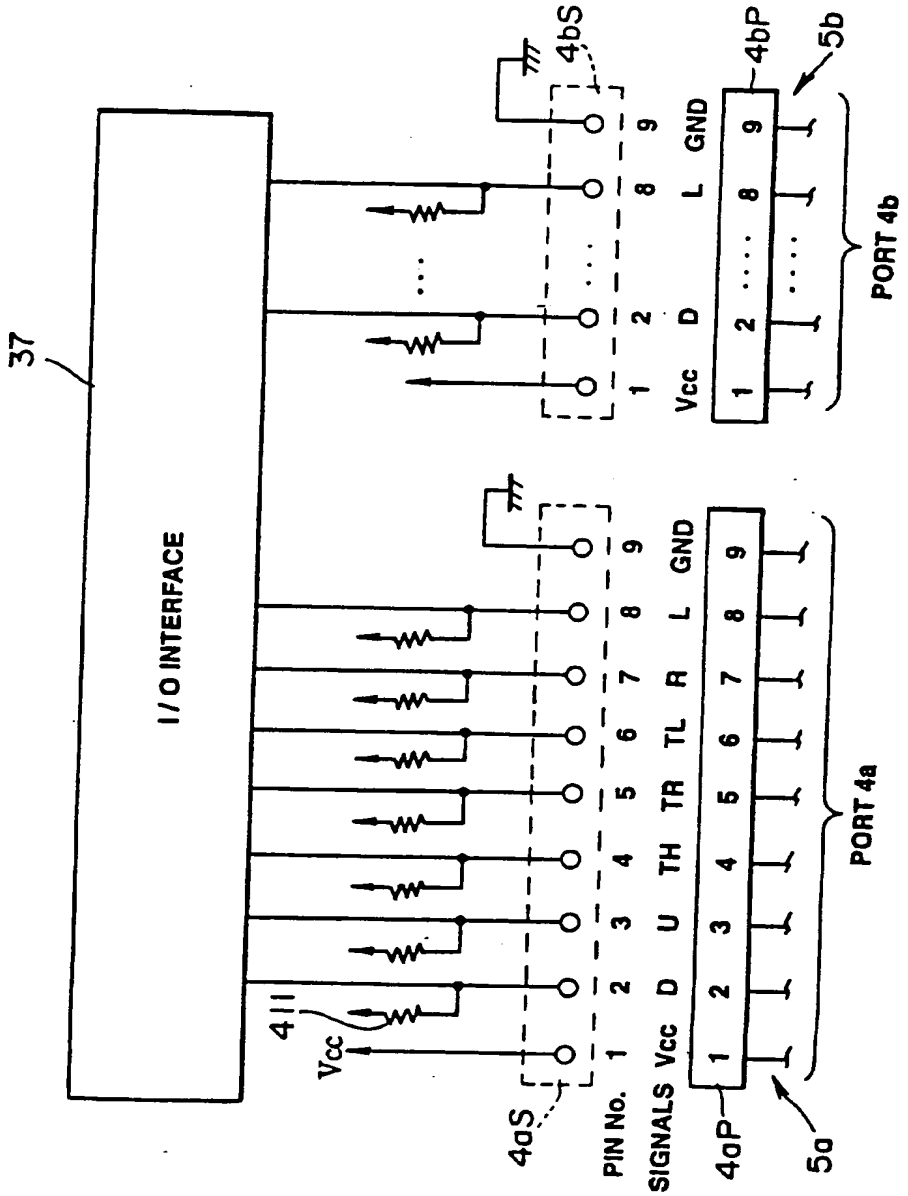

37
I/O INTERFACE
4bS
4bP
5b
PORT 4b
GND
L
D
Vcc
4aS
4aP
5a
PORT 4a
PIN No.
SIGNALS
Vcc
D
U
TH
TR
TL
R
L
GND
411

FIG.4

12:51:44

FIG.5A

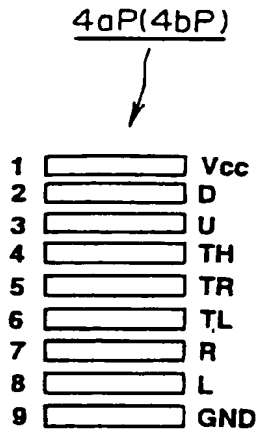


FIG.5B

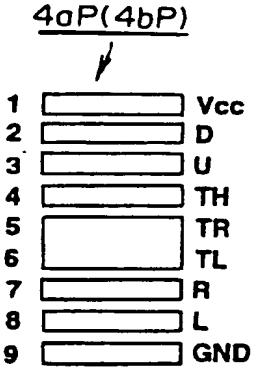
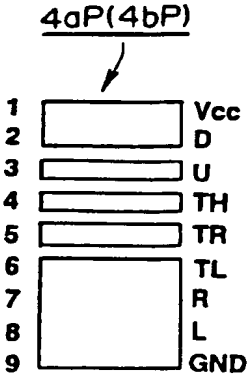


FIG.5C



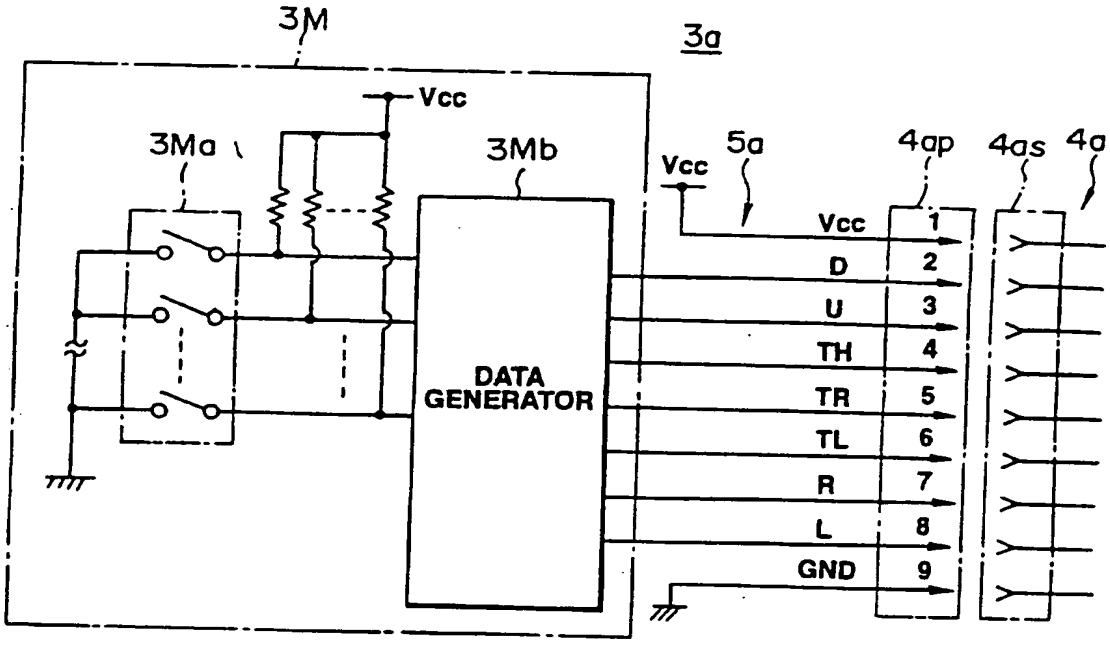


FIG.6A

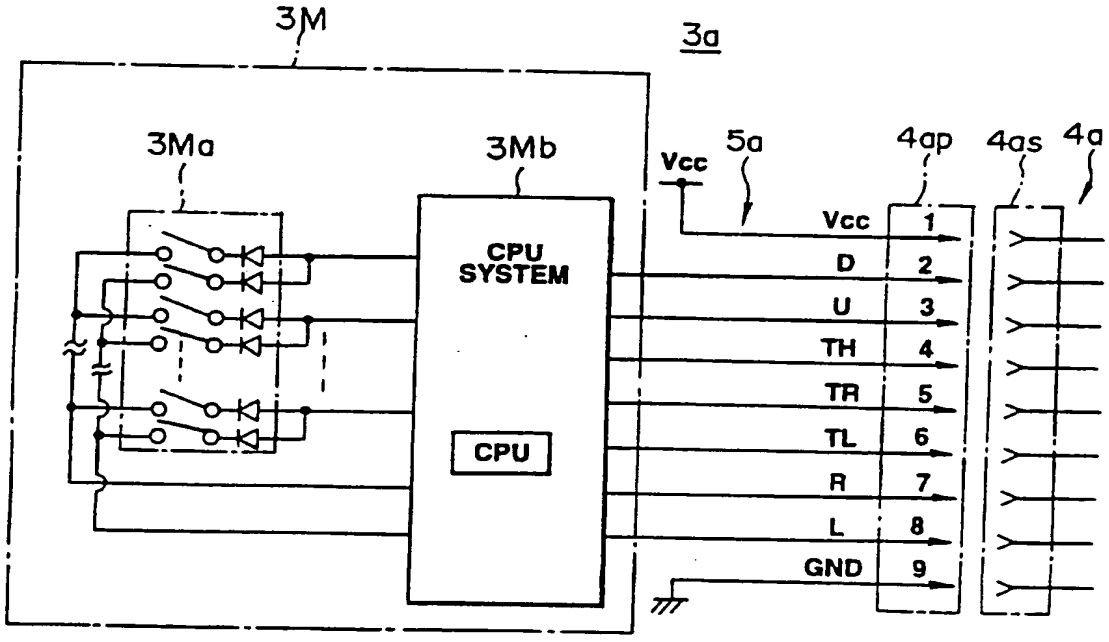


FIG.6B

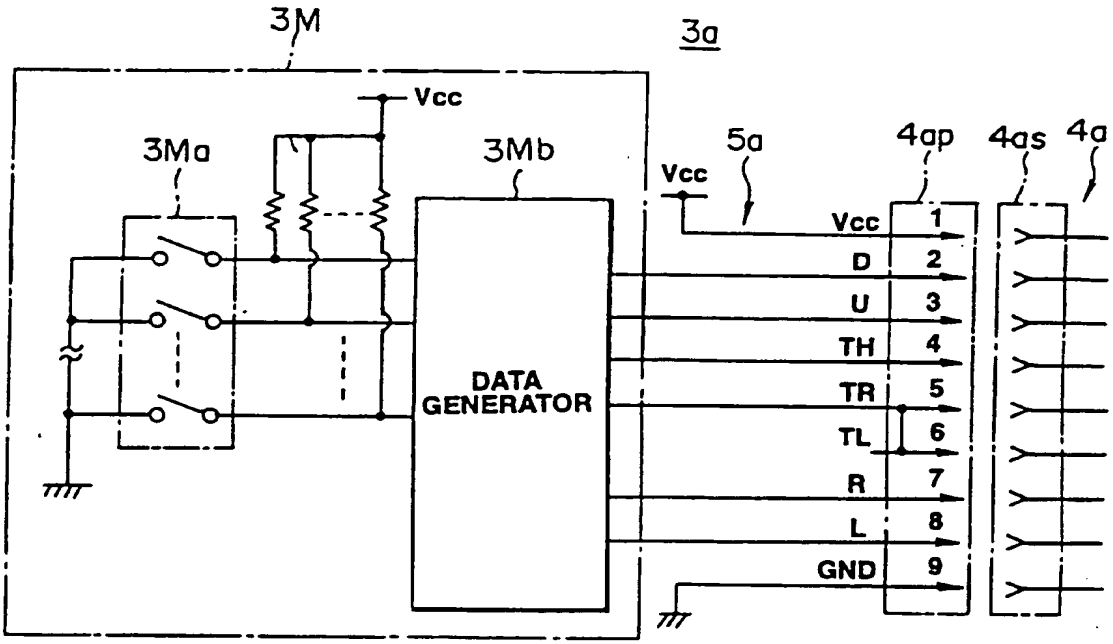


FIG.6C

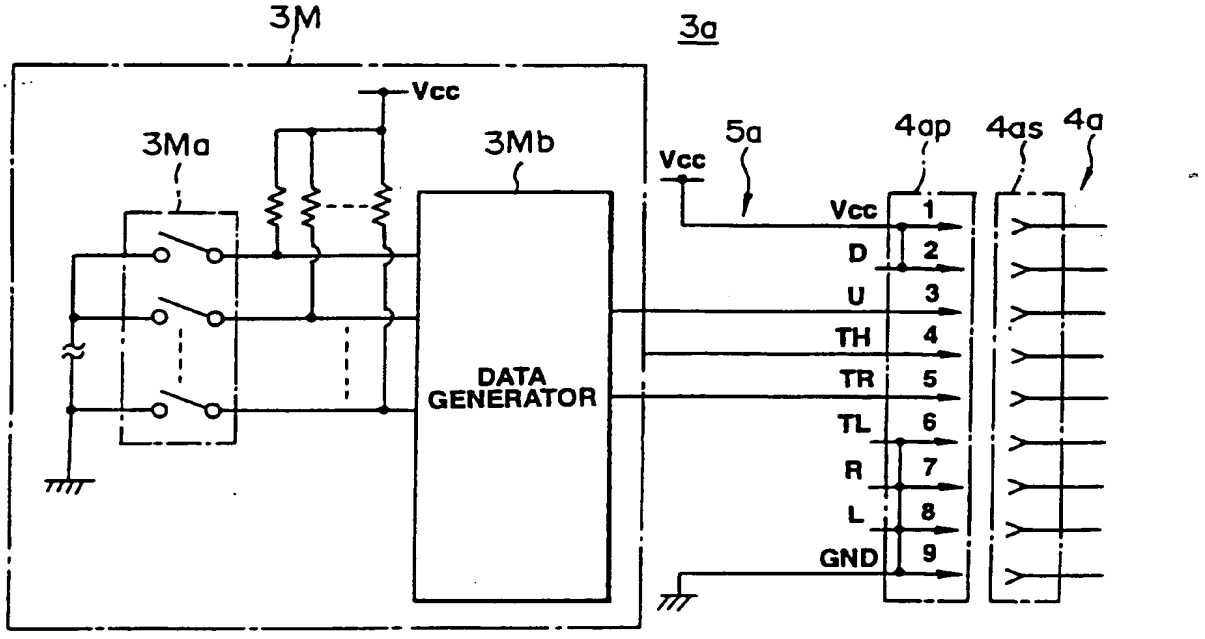


FIG.6D

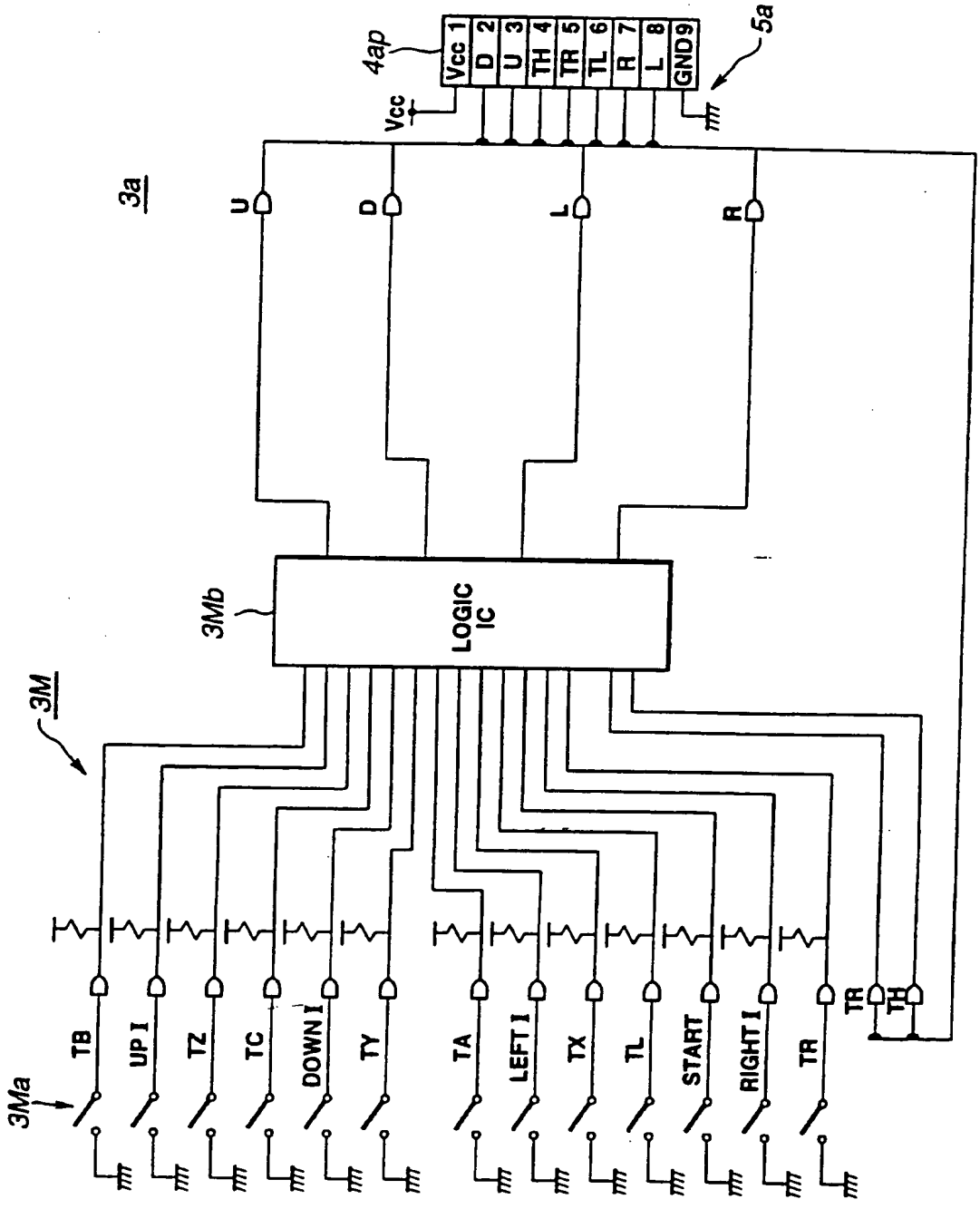


FIG.7A

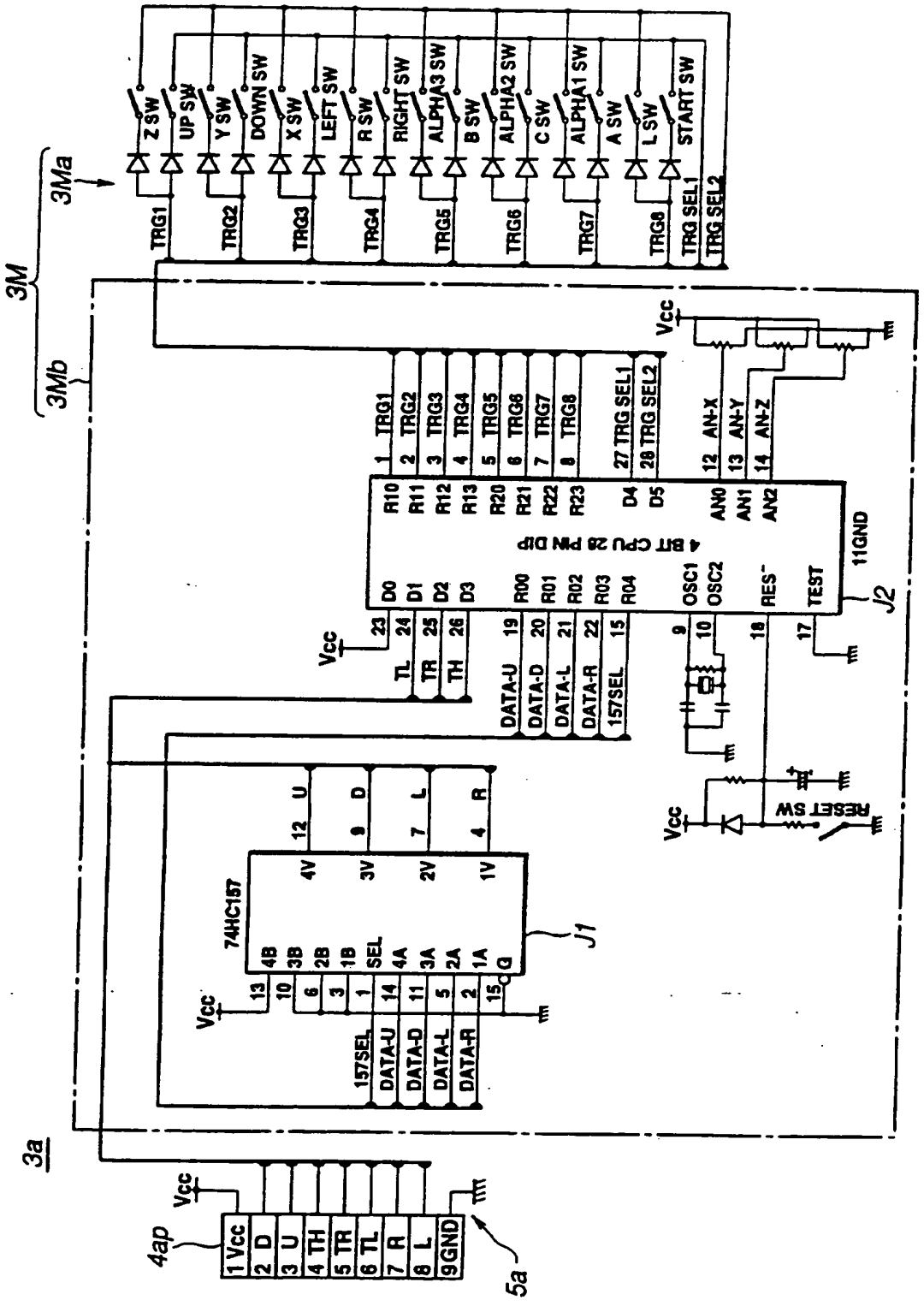


FIG.7B

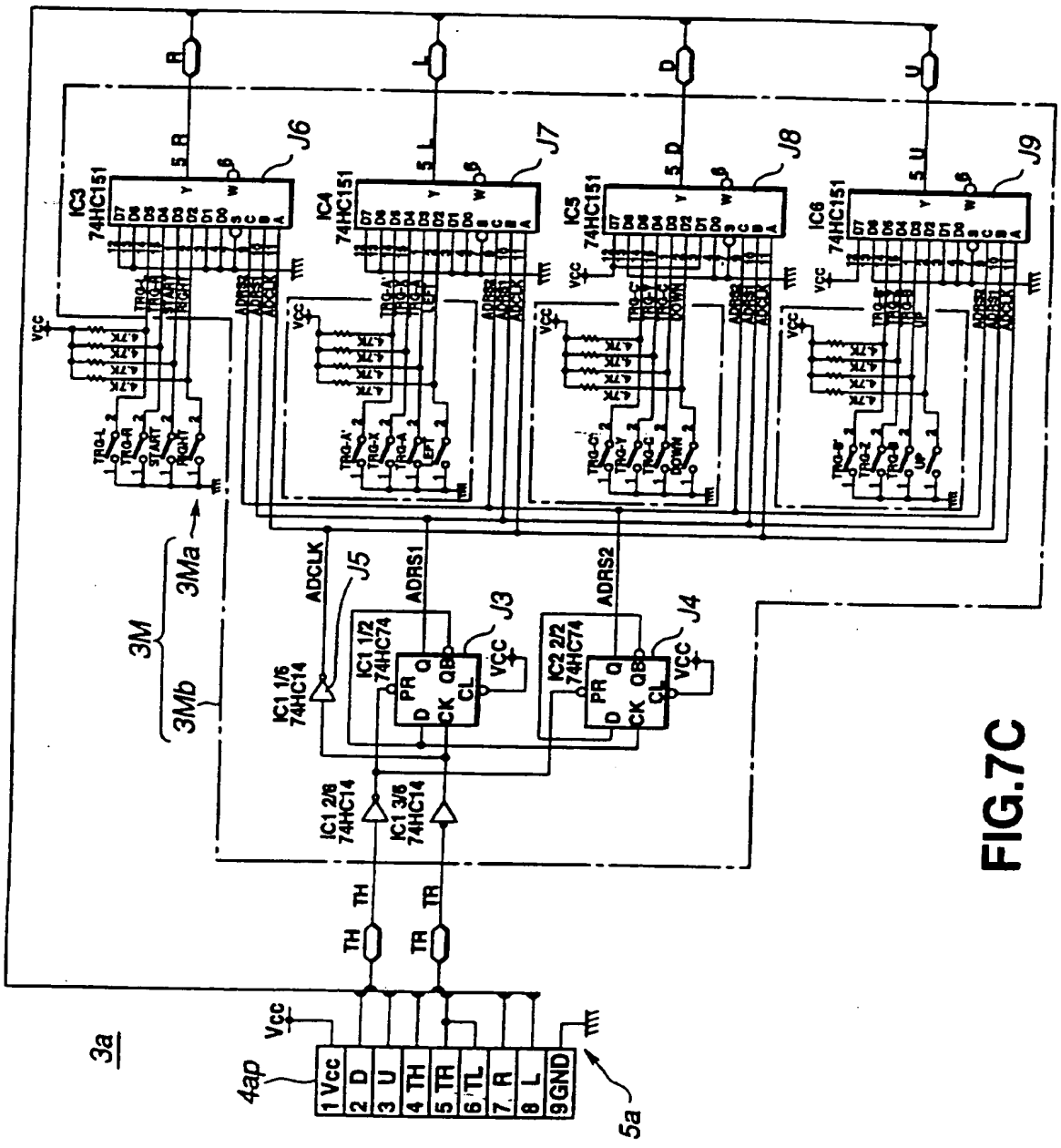


FIG.7C

12:51:44

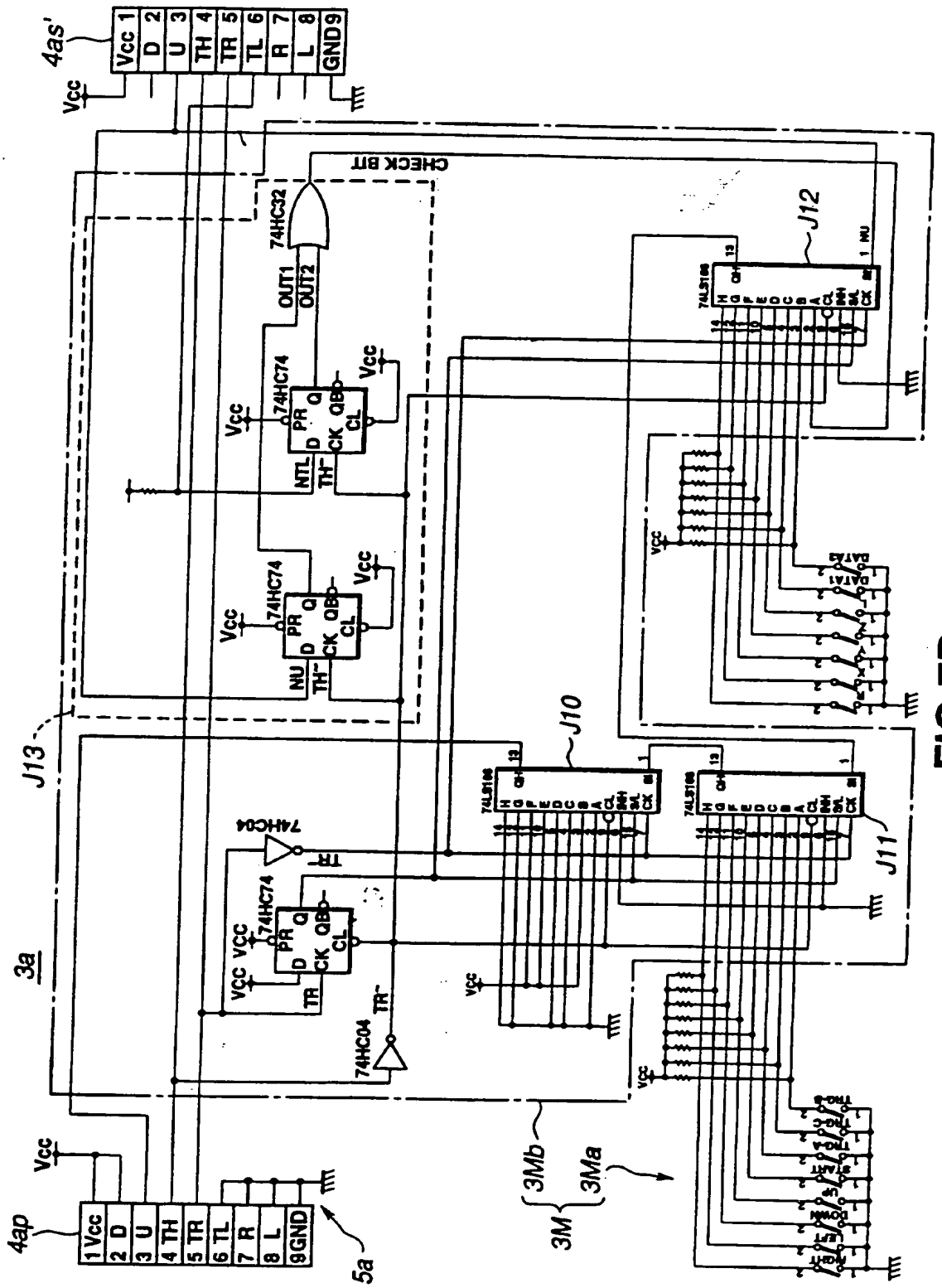


FIG.7D

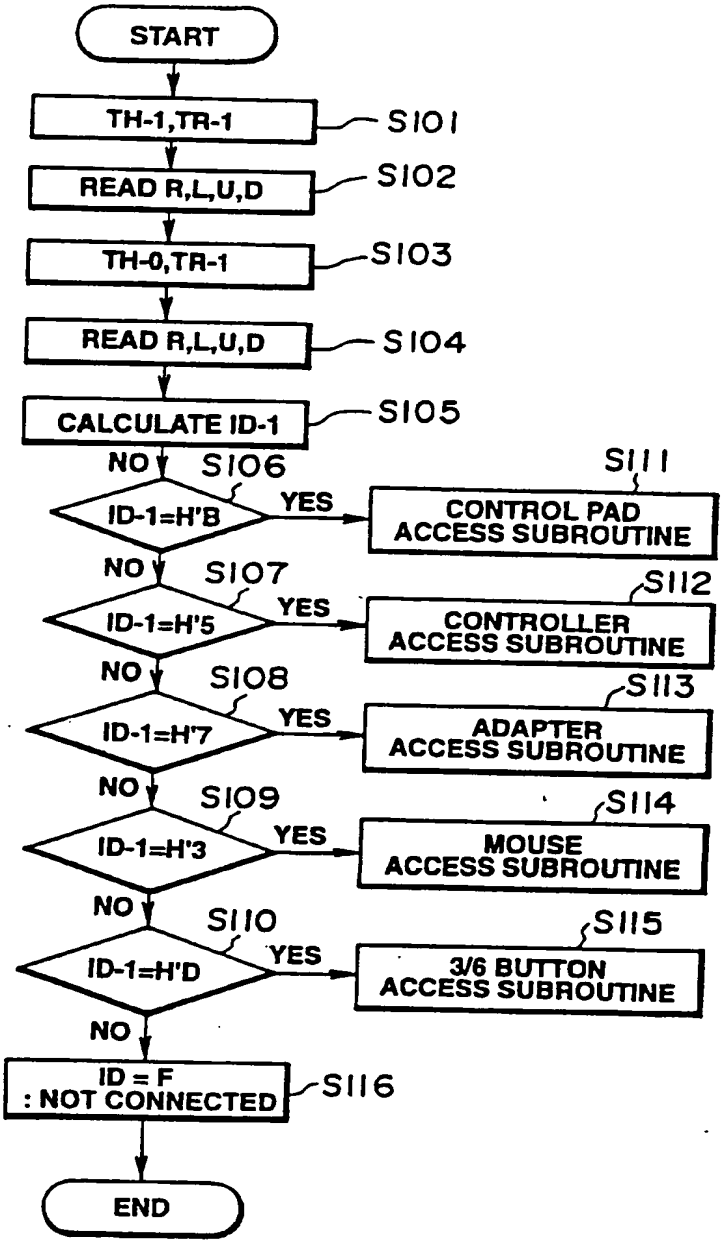

START
TH-1,TR-1
S101
READ R,L,U,D
S102
TH-0,TR-1
S103
READ R,L,U,D
S104
CALCULATE ID-1
S105
NO
S106
ID-1=H'B
YES
S111
CONTROL PAD ACCESS SUBROUTINE
NO
S107
ID-1=H'5
YES
S112
CONTROLLER ACCESS SUBROUTINE
NO
S108
ID-1=H'7
YES
S113
ADAPTER ACCESS SUBROUTINE
NO
S109
ID-1=H'3
YES
S114
MOUSE ACCESS SUBROUTINE
NO
S110
ID-1=H'D
YES
S115
3/6 BUTTON ACCESS SUBROUTINE
NO
ID = F
: NOT CONNECTED
S116
END

FIG.8

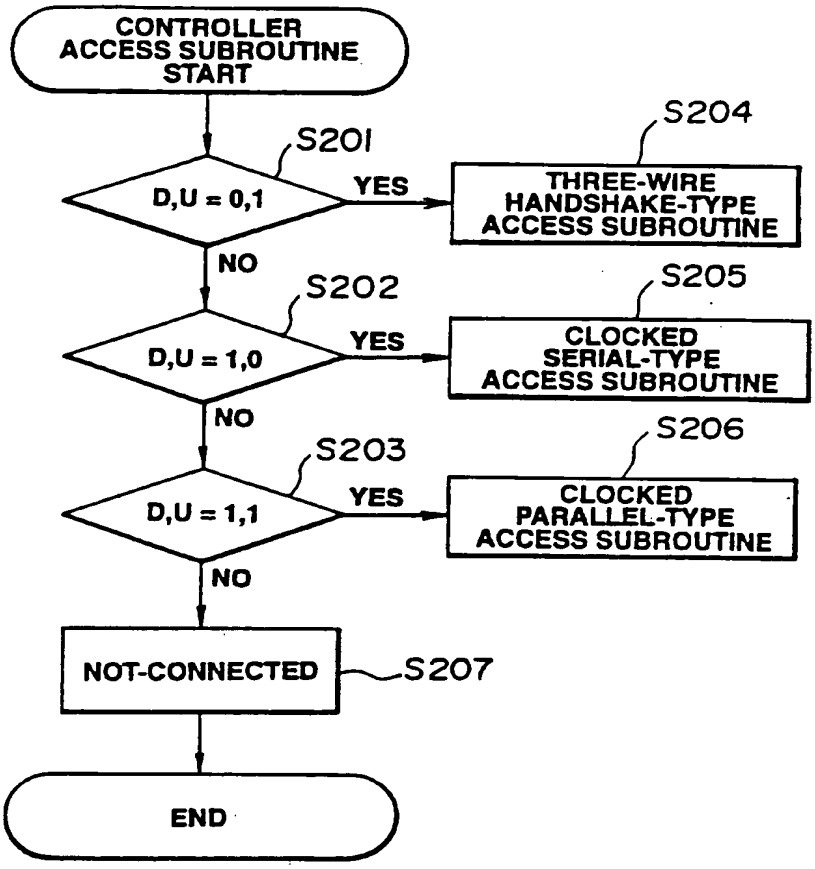

CONTROLLER ACCESS SUBROUTINE START
S201
D,U = 0,1
YES
S204
THREE-WIRE HANDSHAKE-TYPE ACCESS SUBROUTINE
NO
S202
D,U = 1,0
YES
S205
CLOCKED SERIAL-TYPE ACCESS SUBROUTINE
NO
S203
D,U = 1,1
YES
S206
CLOCKED PARALLEL-TYPE ACCESS SUBROUTINE
NO
NOT-CONNECTED
S207
END

FIG.9

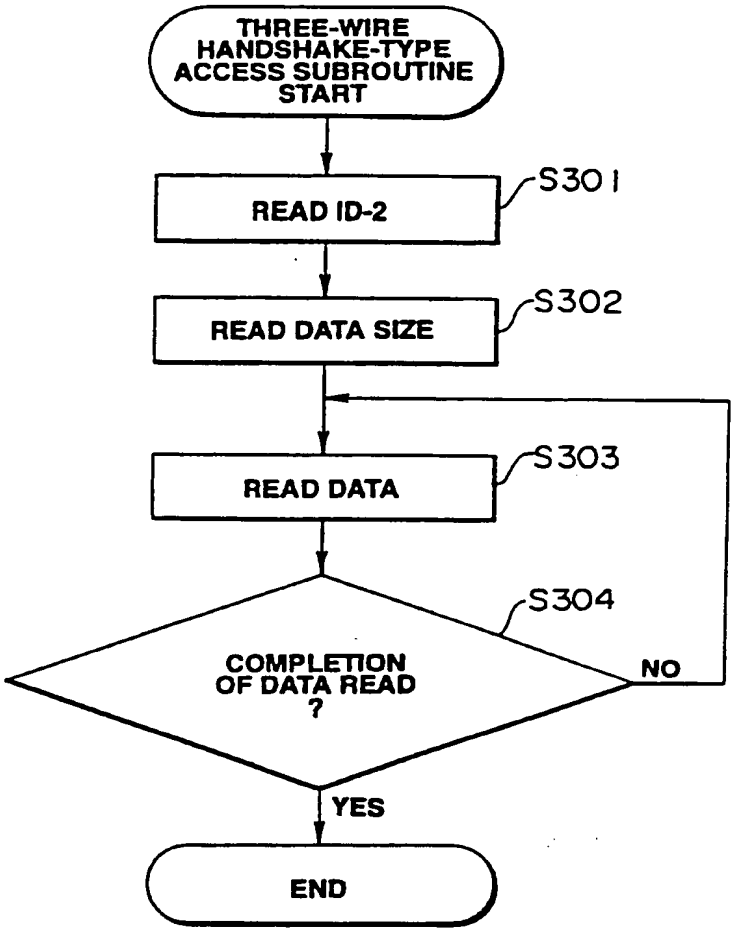


FIG.10

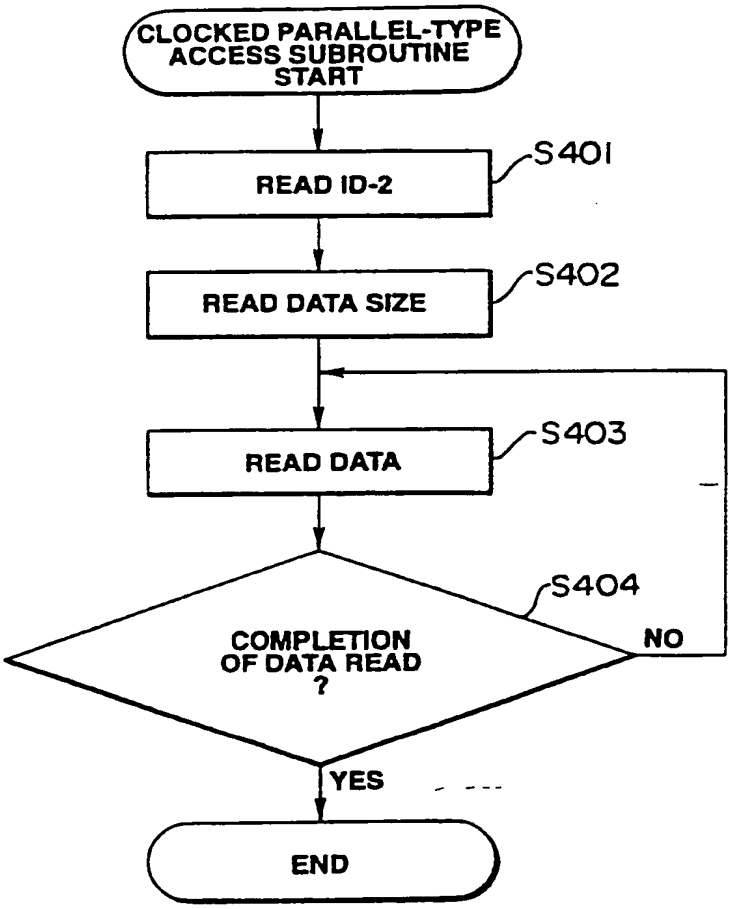


FIG.11

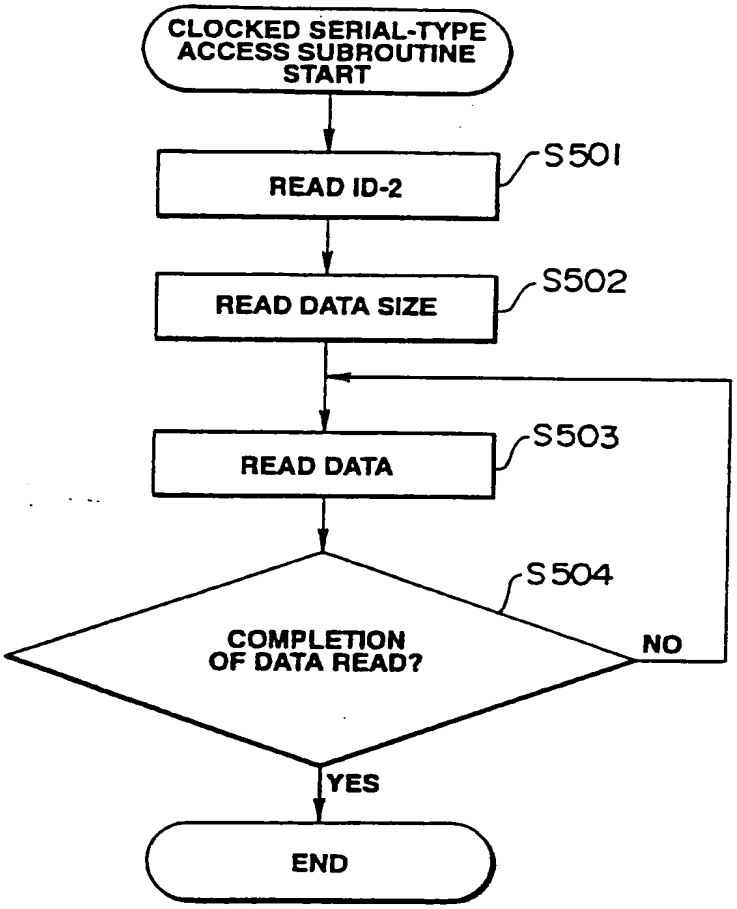


FIG.12

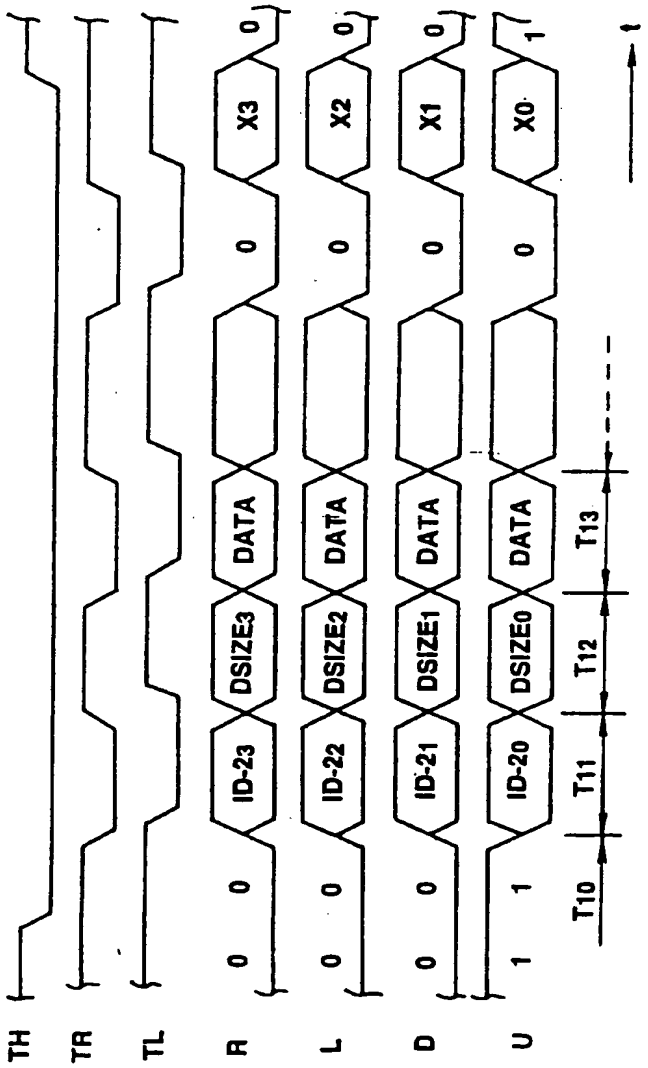


FIG.13

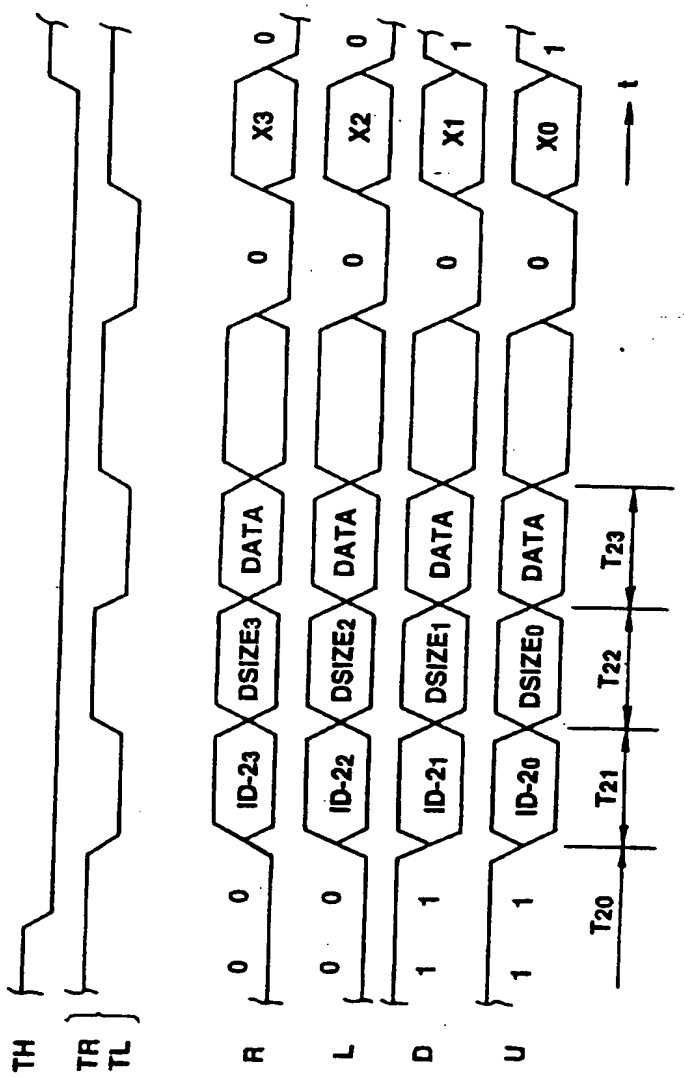


FIG.14

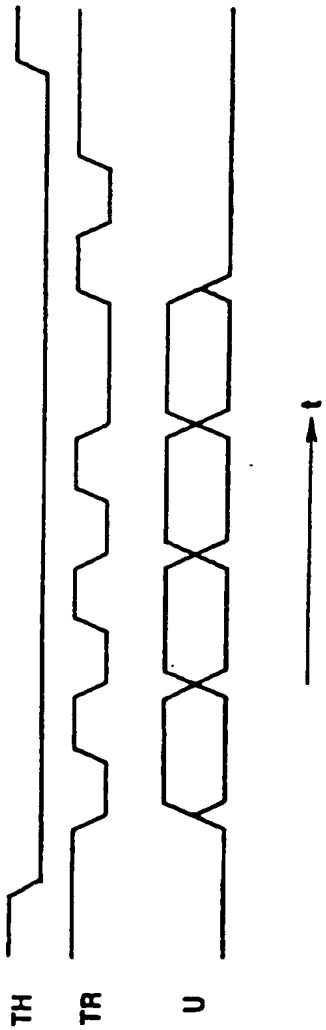


FIG.15

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/JP 95/02073

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06K11/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06K A63F H01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO,A,94 16774 (LIFE FITNESS) 4 August 1994 see figures 1-3,6,7,13 see page 14, line 7 - page 16, line 18 see page 19, line 7 - page 23, line 2 see page 30, line 13 - page 31, line 31	1,2,5,6, 8,11,14, 20, 24-35, 37,42
A	WO,A,88 09573 (CAMBRIDGE COMPUTER LTD.) 1 December 1988 see figures 1,2A,3 see abstract	1,3-13, 20,22, 23,37, 40,42

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 January 1996	09. 02. 96
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Authorized officer Weiss, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

information on patent family members

Int. ional Application No
PCT/JP 95/02073

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A-9416774	04-08-94	AU-B-	3594793	15-08-94
		AU-B-	6024094	15-08-94
		WO-A-	9416777	04-08-94
WO-A-8809573	01-12-88	EP-A-	0362238	11-04-90